PHILCO

A SUBSIDIARY OF *Ford Motor Company*

COMPUTER DIVISION

ELECTRONIC DATA PROCESSING SYSTEMS

PHILCO 2000

INPUT-OUTPUT SYSTEMS

TM-16

PHILCO 2000
INPUT-OUTPUT SYSTEMS

July 1962

PHILCO CORPORATION

A SUBSIDIARY OF Ford Motor Company

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Willow Grove, Pennsylvania

TM—16A

PREFACE

A functional description of the operation of Input-Output Systems and Units of the Philco 2000 Electronic Data Processing System is contained in this manual. Where applicable, simplified block diagrams and flowcharts are also included.

This manual, TM-16A, is a minor revision of TM-16. All changes and corrections issued for TM-16 have been incorporated into this revision.

To permit incorporation of descriptions of new equipment as they become available, this manual has been published in loose-leaf form with each section individually numbered.

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INTRODUCTION TO THE PHILCO 2000 INPUT-OUTPUT SECTION

The Input-Output Section of the Philco 2000 Electronic Data Processing System consists of a group of highly specialized data processing devices that control the transmission of all data into and out of the Central Computer. These devices are individual processing systems whose on-line operation may be initialized either by programmed instructions or by operator intervention at the computer console. With either method, once an order has been accepted by an input-output (I-O) system the Central Computer is released from the transfer operation and is free to continue with the main computer program. For example, during input operations the computer continues with the execution of the program while the I-O system assembles data into full computer words. After each word has been assembled, computer processing is interrupted only for the length of time necessary to transfer that word from the I-O system into memory.

During output operations, computer processing is interrupted only for the length of time required to transfer each full word from memory to the I-O system. The I-O system controls the processing of the word while the computer continues with the execution of the program.

ELEMENTS OF THE INPUT-OUTPUT SECTION

The Input-Output Section contains three major buffer units, five different data recording systems, a Real-Time System, a Digital Information Recorder, Disc File System and an Accounting Clock System. The I-O Section is so designed that any system or unit may be easily installed or removed, depending upon the needs of the specific installation.

The elements of the I-O Section are illustrated in figure INT-1, and their basic function is presented on the following pages. The figure also shows the relationship between elements and their tie-in with the Central Computer.

BUFFER UNITS

The buffer units include an Input-Output Buffer Register (IOB), an Input-Output Processor (IOP), and a Universal Buffer-Controller (UBC).

The IOB

The IOB is a 48-bit register which is used to store one computer word while that word is being written into or read out of the computer memory. This register receives inputs over four different I-O channels and is physically a part of the Central Computer.

The IOP

The IOP is a data processing unit used to couple magnetic tape units and UBC'S to the Central Computer. The IOP accepts inputs and provides outputs over 16 channels and allows data to be transferred over any four of these channels simultaneously.

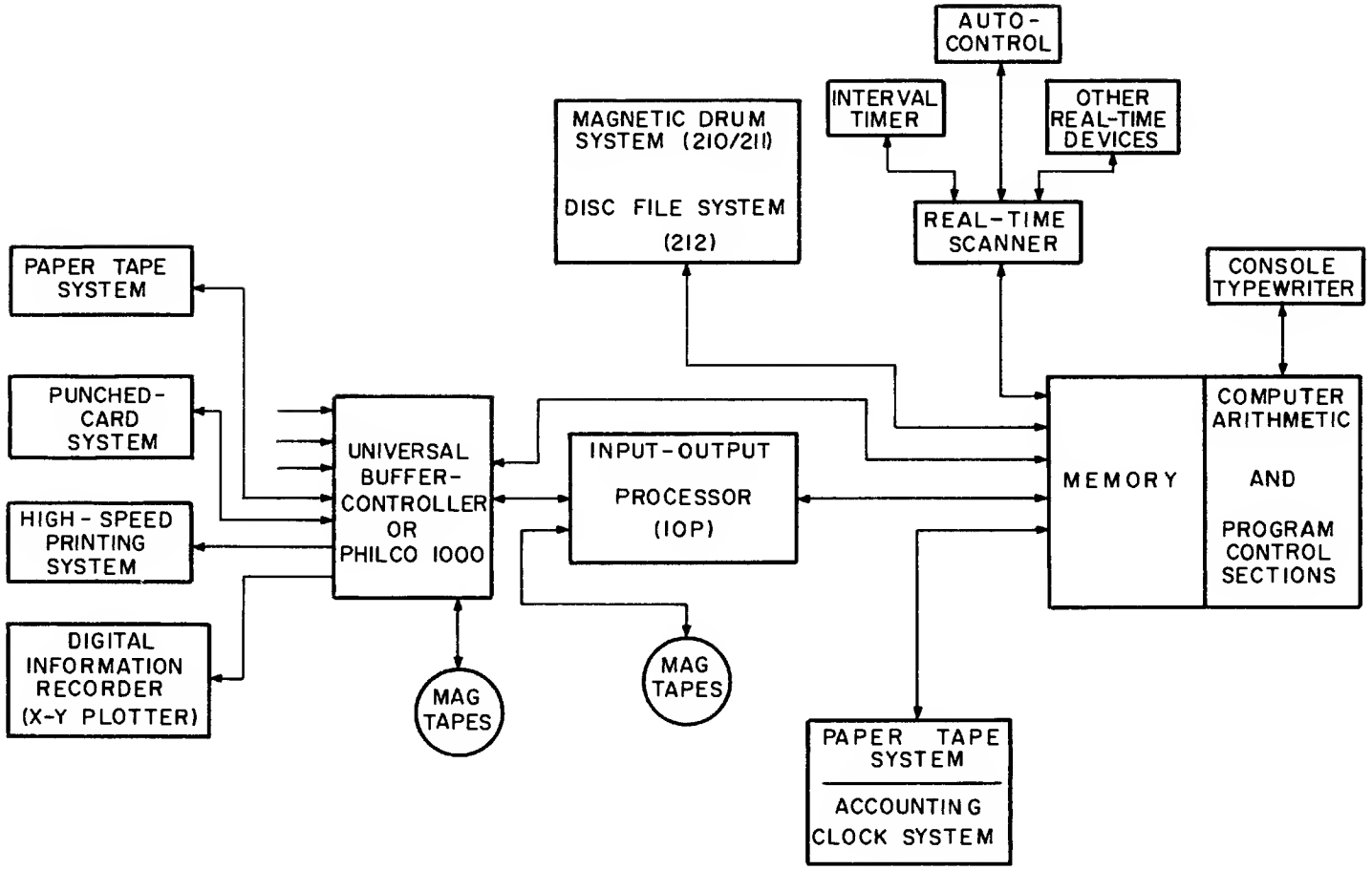

Figure INT-1. Simplified Block Diagram of the Philco 2000 Input-Output Section

The UBC

The UBC provides temporary storage for one block of data (128 words) during on-line operations between the Central Computer and intermediate-speed I-O systems, or during off-line data conversions between any two Philco 2000 I-O media. The I-O systems included in the intermediate speed classification are the Punched-Card and Paper Tape Systems and the High-Speed Printing System.

The UBC has eight data channels which are numbered zero through seven. Channel zero is used exclusively for transferring data to and from the IOP. Channels one and two can be used either for magnetic tape operations or for operations involving the intermediate-speed systems. Channels three through seven are used for the intermediate-speed systems only.

PHILCO 1000 COMPUTER SERIES

The Philco 1000 Computer Series provides stored program computers for installations requiring preformating and post-editing of data for the Philco 2000. A description of the Input-Output equipment in relation to these computers will be found in the Philco 1000 Manual.

RECORDING SYSTEMS

The recording systems include a Paper Tape System, a Punched-Card System, a Magnetic Drum System, a High-Speed Printing System, and a Magnetic Tape System. These systems (with the exception of the printing system, which only records data) provide the means necessary to translate stored data from an I-O medium into electrical pulses which can be used by the computer. In the reverse, they receive electrical pulses from the computer and record them onto an I-O medium. The recorded data can then be stored or used immediately in additional processing operations.

REAL-TIME SYSTEM

The Real-Time System couples any real-time device (radar, teletype, etc.) directly to the Central Computer memory through the IOB. This system includes an Auto-Control Unit with built-in Real-Time Scanner, and an optional Interval Timer Unit.

The Real-Time Scanner multiplexes data from as many as eight real-time devices; the Interval Timer Unit provides a time reference which can be set to facilitate the interlacing of programs; the Auto-Control Unit provides a means of interrupting the main program whenever specified conditions occur in either the Input-Output Section or in the Central Computer.

DIGITAL INFORMATION RECORDER

The Digital Information Recorder is a plotter capable of recording discrete points, continuous curves, letters, numerals, and symbols, based on the output of the Philco 2000. The information to be plotted may come directly from the Central Processor by way of the Universal Buffer-Controller (UBC), or from any input device, such as punched cards, paper tape, or magnetic tape connected to the UBC. Up to four recorders may be coupled to any channel of the UBC.

ACCOUNTING CLOCK SYSTEM

The Accounting Clock System works through the Paper Tape Controller of the Model 240 Paper Tape System, and provides a means of writing into memory at any specified point in the program the month, day, hour, minute, and tenth of a minute for accounting purposes.

DISC FILE SYSTEM

The Philco Disc File System provides a high-speed rapid access storage for the Philco 2000. The Disc File System is connected to the memory of the Central Processor, providing a direct flow of data between the discs and memory without interfering with other input-output operations. An order for data from the disc is transmitted and stored in the Disc File System, allowing the Central Processor to proceed immediately with previously read-in data while concurrently processing the disc order. The input or output of the disc is multiplexed with all other accesses to memory, including High-Performance tapes.

INPUT-OUTPUT CHANNELS

The I-O systems are coupled to the Central Computer memory through the IOB over four different I-O channels, and share memory access time with the Central Computer in a sequence established on a channel priority basis. This means that before each memory request is granted, the Central Computer scans the I-O channels in the established sequence to determine whether or not a previous request has been made from an I-O system operating over a higher priority channel. (It should be noted that the computer memory is accessed each time a word is transferred.)

The order of assigned channel priority and the I-O systems associated with each channel are as follows:

a.	IOP Channel	— One IOP, and any combination of magnetic tape units and UBC'S, up to a total of 16 devices. Of the 16, a maximum of four may be UBC'S.
b.	Real-Time Channel	— Real-Time System
c.	Word-At-A-Time Channel	— One Paper Tape System and one Accounting Clock System
d.	Magnetic Drum or Disc Channel	— Magnetic Drum System (It should be noted that after memory access time is granted during a magnetic drum order, memory cannot be accessed again until the drum order is completed.) On the Philco 212, the Disc File System is used rather than the Drum.

INITIATING INPUT-OUTPUT TRANSMISSIONS

The basic instruction used to initiate the processing of input-output data is the TIO instruction (Transfer Control to Input-Output). When a computer core starting address is required, that memory address is specified by the address portion of the TIO instruction. For example, if the transfer operation were to begin with memory location 1000, the TIO instruction would be written as follows:

LOCATION	COMMAND	ADDRESS AND REMARKS
	TIØ	1000

Basically, the TIO instruction transfers the contents of the D Register to an I-O system. The D Register should contain all the information necessary to perform the transfer operation. This information, which must be prepared before it is placed in the D Register, is called the input-output order. Input-output orders are 48 bits in size, as differentiated from the standard 24-bit computer instruction. As shown in figure INT-2, the D Register is apportioned as follows to contain the parameters of all I-O orders.

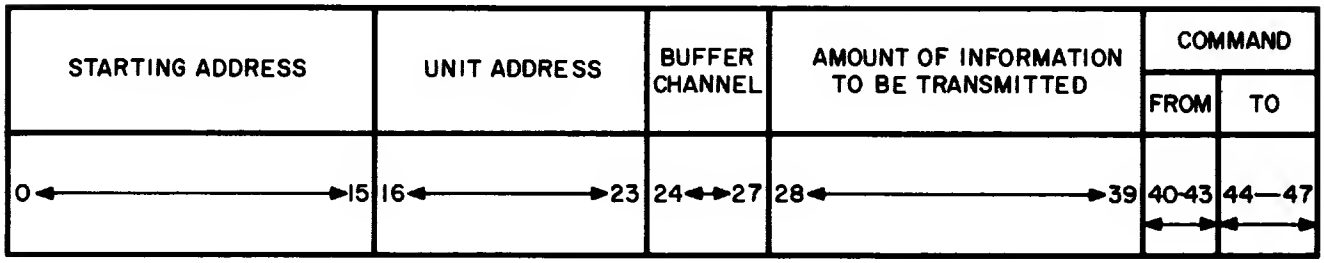

Figure INT-2. Breakdown of D Register Showing Parameters of I-O Order

BITS	CONTENTS
0 through 15	Location of information within the I-O device; the number of blocks to be spaced during magnetic tape operations
16 through 23	IOP channel to which UBC is connected, use bits 20-23; Unit number for real-time devices, use bits 19-22.
24 through 27	UBC channel to which I-O device is connected
28 through 39	Amount of information to be transferred (i.e., number of words, cards, or blocks)
40 through 47	Command — indicates which I-O device is being used. Determines if the order is transferring information to memory from the I-O device, or from memory to the device Bits 40 through 43 indicate device from which data is received. Bits 44 through 47 indicate device to which data is transmitted

ACTION OF THE TIO INSTRUCTION (See figure INT-3.)

Before a TIO instruction can be executed successfully, the parameters of the I-O order must be placed in the D Register. When the TIO is executed, the I-O system designated by the command portion of the order is interrogated to determine whether or not that order can be accepted. If the order can be accepted, the next sequential instruction in the program is skipped. If the order cannot be accepted, the instruction following the TIO is

executed. Two other conditions, in addition to the status of the I-O system, affect the skipping action which follows the execution of the TIO instruction. These conditions are (1) that the command portion of the I-O order has been defined incorrectly and (2) that the I-O order is to the drum system. If the command has not been correctly defined, the next instruction in the program is executed. If the order is to the drum system, the next instruction is always skipped, either after the drum order has been completed successfully, or if it is interrupted because of an error.

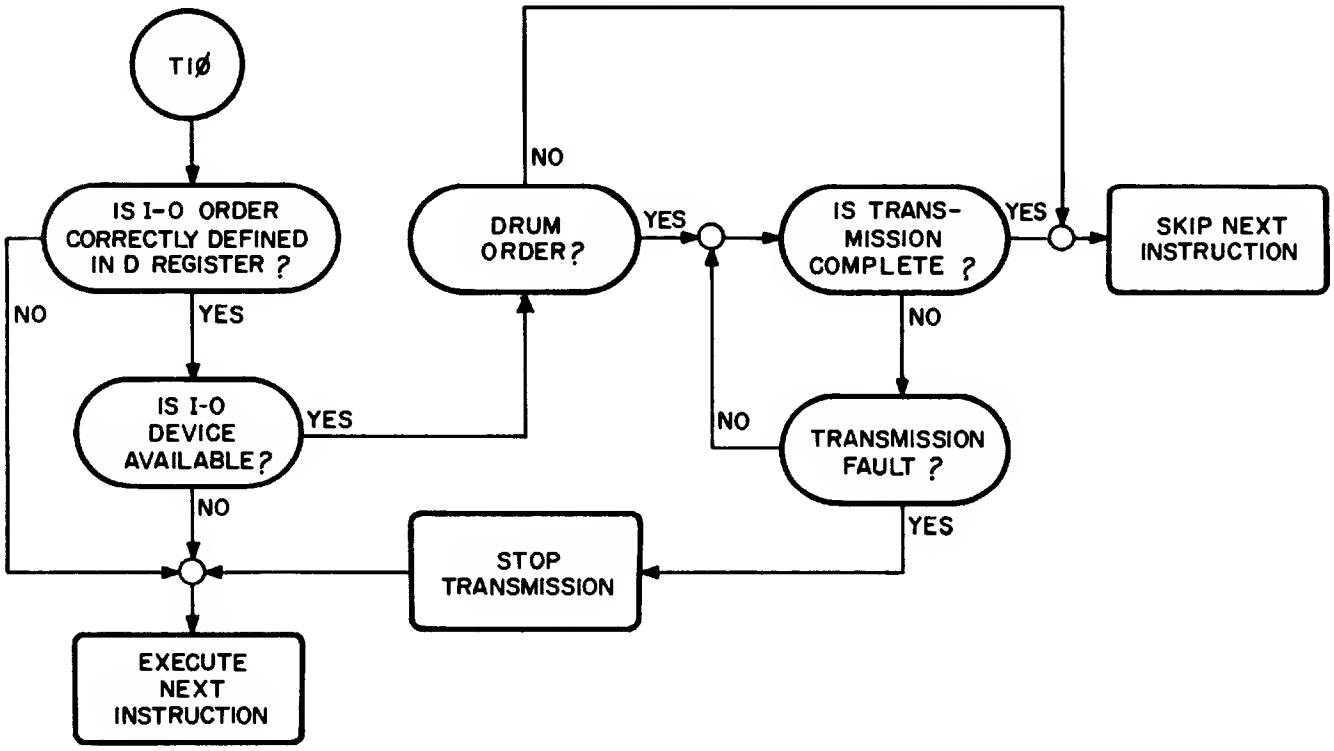

Figure INT-3. Flowchart of the Operations Performed Following the Execution of the TIO Instruction.

SKIP INSTRUCTIONS

Included in the Philco 2000 repertoire of computer instructions are skip instructions, which permit the status of I-O systems and the progress of data transmissions through them to be checked.

In each I-O system there are one or more registers which monitor the action of that system. When the system is busy or if an error is detected during a transmission, a register reflects that condition. Essentially, skip instructions are used to check the contents of these "information" registers.

EXAMPLE OF I-O CODING

The following instructions illustrate how the I-O order and computer instructions could be written to initiate I-O operations:

LOCATION	COMMAND	ADDRESS AND REMARKS
	TMD	I-O ORDER
	TIØ	1000
	JMP	DIAGNO
PROCESS	AM	XXXX
	.	
	.	
	.	
DIAGNO	XXX	XXXX

The TMD instruction transfers the I-O order from memory into the D Register; the TIO instruction is used to execute that order. If the order is acceptable, the jump instruction is skipped and the instruction at location PROCESS is executed. If the order is not acceptable, the jump to DIAGNO is executed. Starting at location DIAGNO, a series of skip instructions could be used to determine why the order was not accepted.

GENERAL OPERATION OF THE INPUT-OUTPUT SECTION

Since the I-O systems process data independently of the Central Computer operation, two different I-O systems may be used concurrently, one processing input data and the other processing output data. In actual operation, as many as nine systems may be processing data concurrently. Of the nine, some may be processing input data while the remaining systems are processing output data. Conditions may also exist where all the systems may be processing either input or output data.

Two systems are used in an illustration to describe the operation of the input-output systems with the Philco 2000 Computer. (See figure INT-4.) In the following description, Unit 1 is used for the input operation, Unit 2 is used for the output operation, and the I-O order is assumed as being accepted:

a. During the main computer program, the parameters of the input order are transferred to the designated input-output system (Unit 1).

b. The Central Computer continues with the main program and Unit 1 processes the input data. Processing includes assembling the information into full words, checking the accuracy of the transmission, and storing the assembled words in a register.

c. Later in the main program, the parameters of an output operation which involves Unit 2 are transferred to that device, and the first word to be transmitted is transferred from the Central Computer to Unit 2.

d. The Central Computer returns to the main program, and the Input-Output Section simultaneously processes both the first word of the output operation and the first word of the input operation. The processing of the output operation includes checking the transmission, altering the data format, and recording the information on the specified recording device.

e. When Unit 1 has formed one full word, the word is stored in a register and a signal is sent to the Central Computer. This signal indicates that a word is ready to be written into memory.

f. When the computer memory is available, the Central Computer sends a signal which indicates that the word from Unit 1 can now be written into memory.

g. After the word from Unit 1 is written into memory, Unit 1 starts to process the next input word, and Unit 2 continues to process the first output word.

h. When Unit 2 has completed processing one word, a signal is sent to the Central Computer which indicates that the next word can be accepted.

i. When memory is available, the Central Computer transfers the second word of output information to Unit 2.

j. The Central Computer then returns to the main program, and the two input-output systems continue to process data. The cycle (steps d through i) is repeated until all input-output data is processed.

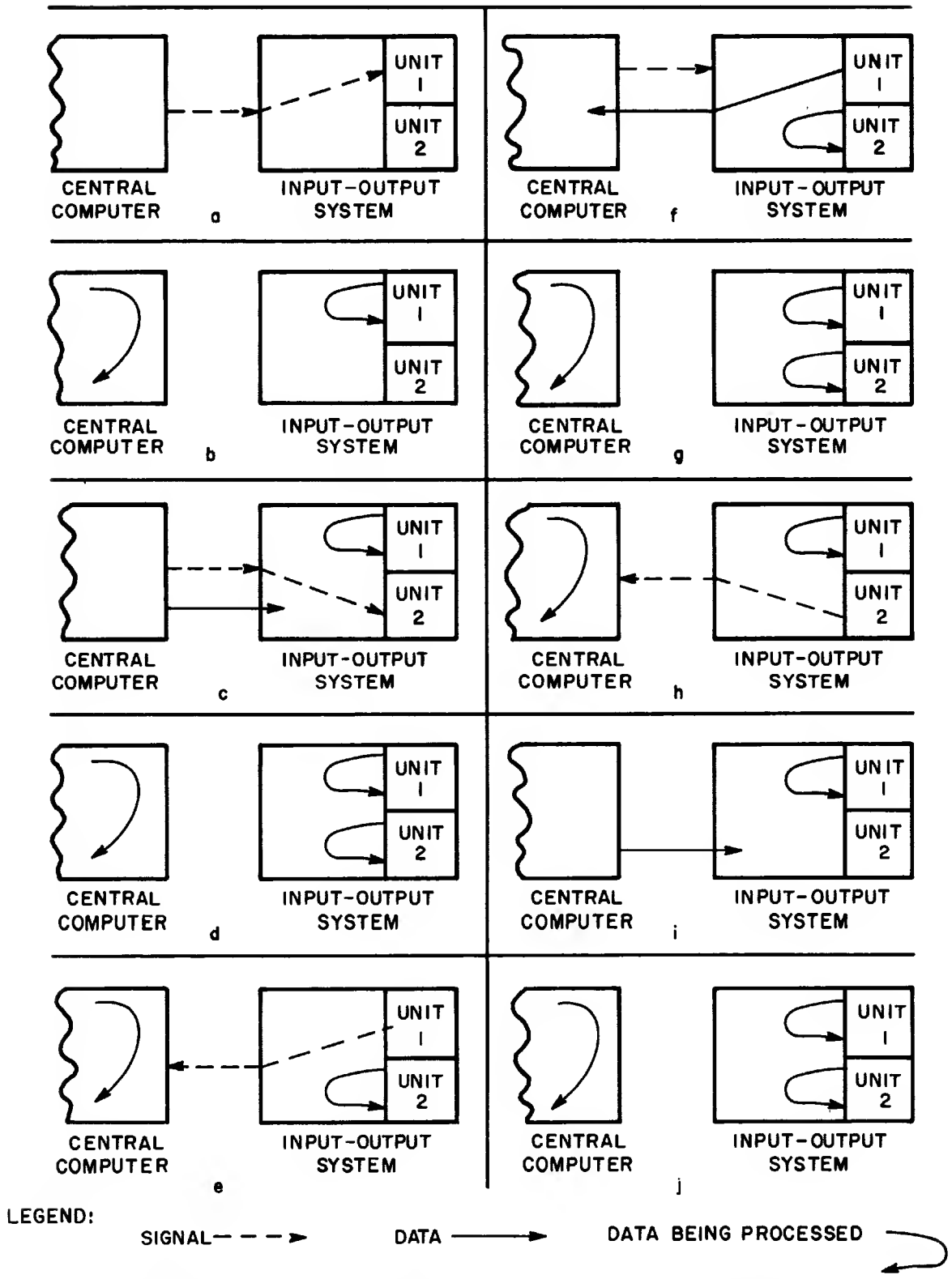

Figure INT-4. General Operation of the Input-Output System

PHILCO 2000 CODE COMBINATIONS

A total of 64 discrete characters comprise the list of the Philco 2000 Code Combinations. These characters are shown in figure INT-5, and also on form TF17. In the figure, columns one and five contain the 64 "human language" numbers, letters, and symbols. Columns two and six contain the octal equivalent of the binary code for these characters. Columns three, four, seven, and eight list the associated Hollerith punch and Console Typewriter key.

PHILCO® 2000 CODE COMBINATIONS

Philco Character	Octal Code	Hollerith Punch	Console Typewriter	
			Upper	Lower
0	00	0	0	?
1	01	1	1	<
2	02	2	2	;
3	03	3	3	e
4	04	4	4	$
5	05	5	5	@
6	06	6	6	(
7	07	7	7	>
8	10	8	8	'
9	11	9	9	#
@	12	8-2 ①	(See LC 5) ②	
=	13	8-3	=	"
;	14	8-4	(See LC 2) ②	
≡	15	8-5 ①	(See LC &) ②	
&	16	8-6 ①	&	≡
'	17	8-7	(See LC 8) ②	
+	20	12	+	*
A	21	12-1	A	a
B	22	12-2	B	b
C	23	12-3	C	c
D	24	12-4	D	d
E	25	12-5	E	e
F	26	12-6	F	f
G	27	12-7	G	g
H	30	12-8	H	h
I	31	12-9	I	i
n ③	32	12-8-2 ①	CAR. RET.	
.	33	12-8-3	:	
)	34	12-8-4	(See LC %) ②	
%	35	12-8-5 ①	%	)
?	36	12-8-6 ①	(See LC 0) ②	
"	37	12-8-7 ①	SHIFT UPPER	

Philco Character	Octal Code	Hollerith Punch	Console Typewriter	
			Upper	Lower
-	40	11	-	/
J	41	11-1	J	j
K	42	11-2	K	k
L	43	11-3	L	l
M	44	11-4	M	m
N	45	11-5	N	n
O	46	11-6	O	o
P	47	11-7	P	p
Q	50	11-8	Q	q
R	51	11-9	R	r
¬	52	11-8-2 ①	TAB	TAB
$	53	11-8-3	(See LC 4) ②	
*	54	11-8-4	(See LC +) ②	
<	55	11-8-5 ①	(See LC 1) ②	
#	56	11-8-6 ①	(See LC 9) ②	
⊔	57	11-8-7 ①	SHIFT LOWER	
Δ ③	60	Blank ⑤	SPACE	
/	61	0-1	(See LC -) ②	
S	62	0-2	S	s
T	63	0-3	T	t
U	64	0-4	U	u
V	65	0-5	V	v
W	66	0-6	W	w
X	67	0-7	X	x
Y	70	0-8	Y	y
Z	71	0-9	Z	z
|	72	0-8-2 ①	STOP CODE	
,	73	0-8-3		⊔
(	74	0-8-4	(See LC 6) ②	
>	75	0-8-5 ①	(See LC 7) ②	
:	76	0-8-6 ①	(See LC .) ②	
e ③	77	0-8-7 ①	DELETE CODE	

CONTROL CHARACTERS

Character	Console Typewriter	High-Speed Printer	Punched-Card System
n	Carriage Return	Null	Null
¬	Tab	Cond. Stop ④, Prints ¬	Cond. Stop ④, End of Block
Δ	Space	Space	Blank Column ⑤
|	Stop Code	Abs. Stop ④, Prints |	Abs. Stop ④, Punches 0-8-2
e	Delete Code	End of Line	End of Card
"	Shift to upper case	Prints "	Punches 12-8-7
⊔	Shift to lower case	Prints ⊔ (logical OR)	Punches 11-8-7

NOTES

① These codes can be punched on the keypunch by multiple punching.

② The octal codes for these Philco Characters are illegitimate on the Console Typewriter. To type these characters from the computer, first transmit a shift to lower case (octal code 57), then transmit code for Philco character indicated in parenthesis.

③ These characters are printed by the Line Printer when in Write - All mode only.

④ These characters are recognized only when the second character in a block in off-line non-data select operation; otherwise second function is performed.

⑤ A switch on the Punched-Card Controller allows blank columns to be read as Philco Character 0 or Δ

TF17(7-61)

PHILCO® 2000

Figure INT-5. Philco 2000 Code Combinations

MAGNETIC TAPE

INTRODUCTION

Magnetic tape provides the principal input-output medium for the Philco 2000 System, and the tape transports are the fastest commercially available tape recording devices.

Data is recorded on magnetic tape in blocks of 128 words and may be processed either one block at a time, or in multiples thereof, to a maximum of 16 blocks per I-O order. This arrangement of data on tape is shown in figure MT-1.

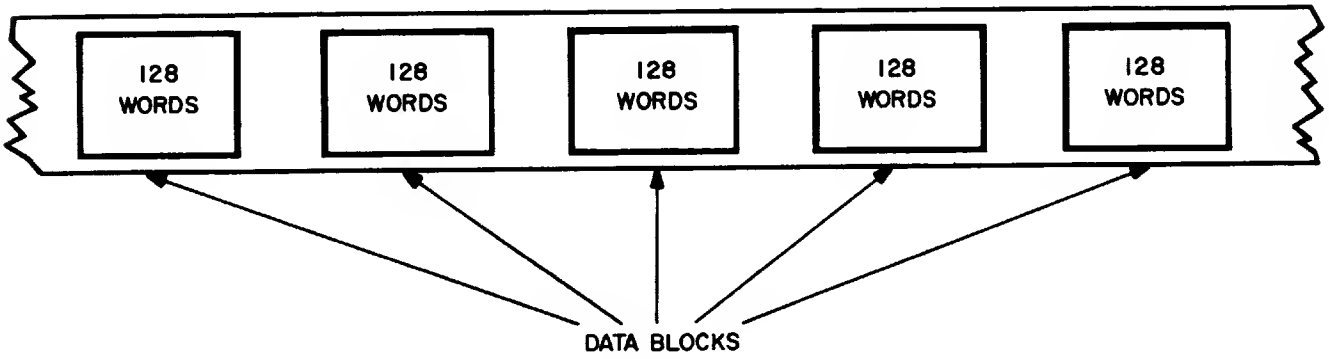

Figure MT-1. Arrangement of Data on Magnetic Tape

DATA FORMAT (See figure MT-2)

In the Philco 2000 alphanumeric code, a computer word (48 bits) is represented by eight units of six-bits each. These units are called "characters." The characters are recorded two at a time across the width of the tape, and each pair is called a "frame." In turn, the data frames are recorded in groups of 512, and each group is referred to as a "block."

In addition to the two characters in each frame, two checking bits, called "parity" bits, are also recorded. One parity bit is recorded for each character. The value of the parity bit is chosen so that the total number of "one" bits in the seven bits recorded for each character is always odd. Parity bits are used to check the accuracy of data transmission.

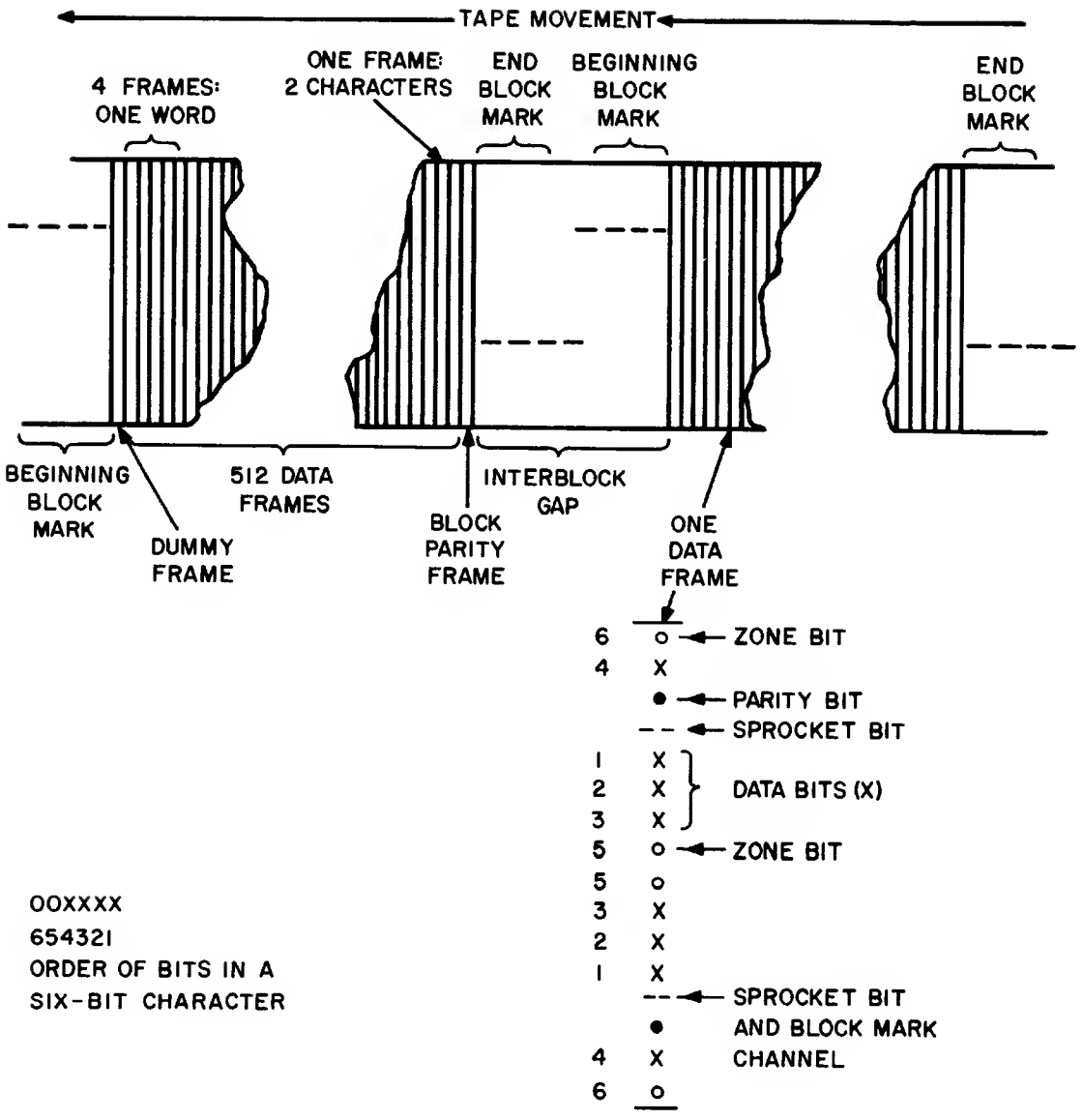

Figure MT-2. Magnetic Tape Format

Each frame is followed by two sprocket marks, one sprocket mark following each character in the frame. The sprocket marks are used to indicate tape skew and to provide a means of counting the total number of frames in a block.

The bits of each character in the frame are recorded in a particular arrangement. Starting at either side of the tape and moving toward the center, the pattern of bits for one character is as follows: 6, 4, parity, sprocket, 1, 2, 3, and 5. Six represents the most significant bit, and 1 represents the least significant bit of the six-bit Philco 2000 character.

The total number of frames in each block is 514. A block consists of 512 data frames, a channel parity frame, and a dummy frame. The channel parity frame is recorded following the last data frame. In the channel parity frame, the value of each bit is chosen so that an even number of "one" bits exists for each channel in the block. (Channels are the areas of tape on which data is recorded. One data channel covers the length of the tape, and 16 data channels cover its width.)

The dummy frame is recorded preceding the data frames. It contains all "zeros," with the exception of the parity bit recorded for each character; "ones" are recorded in these bit positions. The purpose of the dummy frame is to simplify control by providing a symmetrical format in the recording areas of the tape. With 514 frames, the first and last frames are not data frames, regardless of the direction of the tape movement.

Although there are 514 frames in each block, the total number of sprocket mark pairs recorded in each block is 515. A pair of sprocket marks is recorded preceding the dummy frame in each block to provide a means of checking tape skew when the tape is being read in the backward direction.

BLOCK MARKS

Each block is bracketed by block marks, which denote the areas on tape in which data can be recorded. The block marks which precede the block are called Beginning Block Marks (BBM's), and those which follow the block are called Ending Block Marks (EBM's).

There are 16 magnetic pulses comprising the BBM's and 17 magnetic pulses comprising the EBM's. The pulses of the BBM's are recorded preceding the sprocket mark in channel 13, and the pulses of the EBM's are recorded following the sprocket mark in channel 4. Block mark pulses are differentiated from sprocket marks in that they are recorded at twice the density of sprocket marks; that is, twice as many block mark pulses appear in the same area of tape.

Block mark pulses are also used to indicate when a tape has deteriorated beyond the point at which information can be recorded or read reliably. Usable areas of tape are identified by the presence of a minimum of eight continuous block mark pulses. If there are less than eight continuous pulses, a missing block mark condition is present. If there are more than eight but less than 12 continuous pulses, an improper block mark condition is present. Any number of continuous pulses of more than 12 is treated as a proper block mark. These block mark conditions are displayed on the control panel of the IOP.

INTER-BLOCK GAP

The inter-block gap is the area between two adjacent blocks, and it includes both block marks and an information free area. The information free area between block marks is used for starting and stopping the tape.

ACCEPTANCE OF MAGNETIC TAPE ORDERS

The acceptance of magnetic tape orders is controlled by the IOP, and the procedure which is followed is described in the chapter dealing with the IOP.

TAPE OPERATION

In the magnetic tape unit there are 16 read heads and 16 write heads. One read head and one write head are used in each of the 16 data channels of the tape. When tape is moved

in the forward direction, the tape passes under the write head first. This order is established to permit the read-back of information during a writing operation so that the accuracy of each recording may be checked.

WRITING ON TAPE

During a write operation, the IOP receives the data from the Central Computer memory and transfers a maximum of 16 pulses in parallel to the write heads. A pulse, when present, changes the direction of the magnetic field created by the write head and causes a "one" to be recorded.

The characters of each computer word are recorded in a particular arrangement on the tape. As shown in figure MT-3, all even characters of the computer word are recorded on one side of the tape and all odd characters are recorded on the other.

READING TAPE

During a read operation, any change in the magnetic field on the surface of the tape passing under the read heads is interpreted as a "one." The output from the 16 read heads is transferred in parallel to the IOP. The IOP, in turn, transfers the information to the Central Computer memory.

WRITE ENABLE RING

The write enable ring is a safety feature which guards against the loss of data resulting from unintentional recording on or erasing of a particular tape. All tape reels are equipped with this removable ring, and without the ring, data cannot be recorded. With or without the ring, however, data can be read.

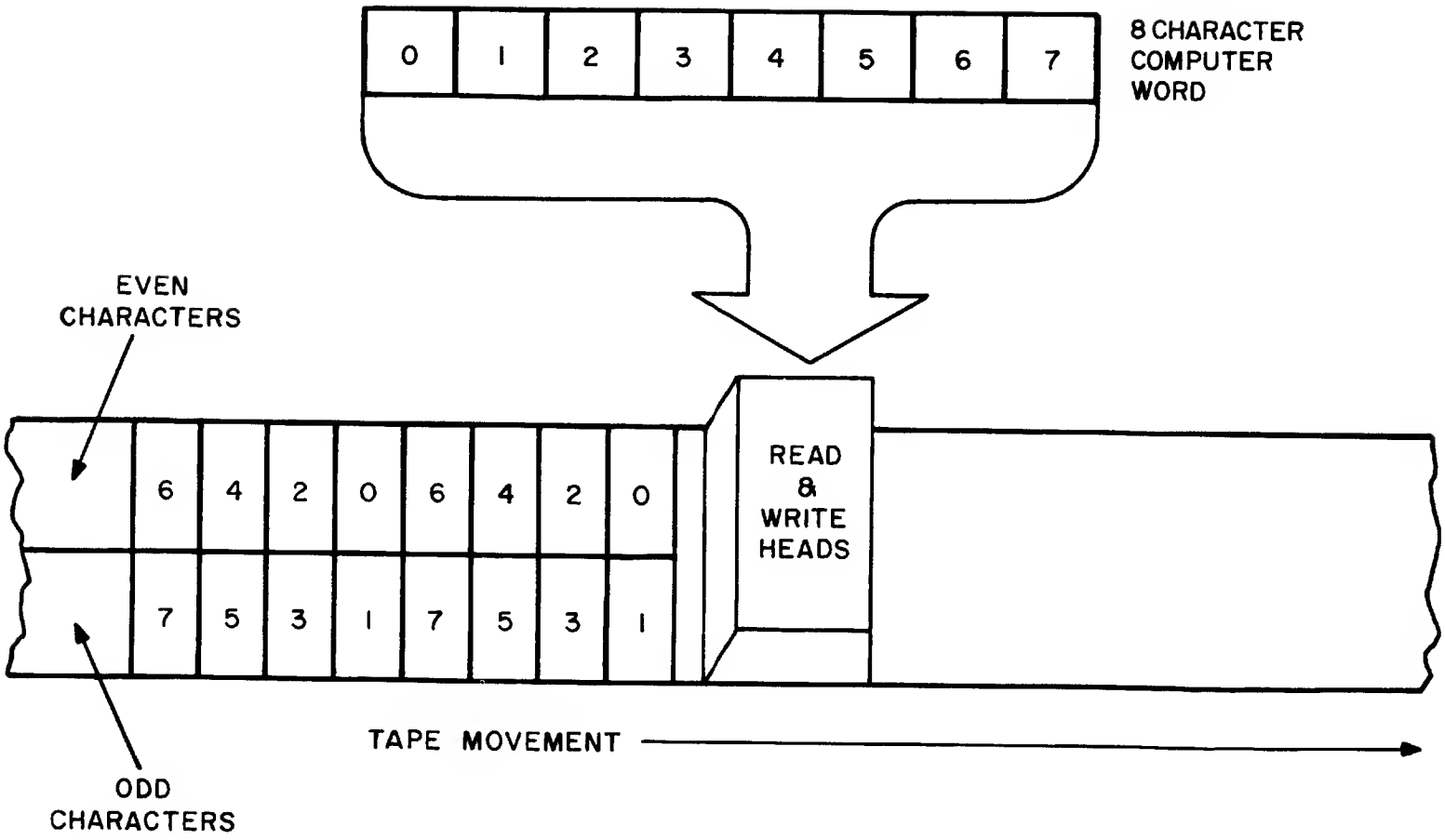

Figure MT-3. Arrangement of Characters on Tape

PHYSICAL CHARACTERISTICS OF TAPE

The magnetic tape has a Mylar* base and is one inch wide and one mil thick. The beginning and end of every reel is coated with a non-plastic sensitized material (silver); when this sensitized area is detected, the tape stops automatically.

Tapes are furnished in lengths of 600, 2400, or 3600 feet per reel.

OPERATING CHARACTERISTICS

a. Read/write speeds of 90,000 alphanumeric characters per second
b. Recording density of 750 alphanumeric characters per inch
c. Tape speed of 120 inches per second
d. Tape rewind speed of 180 inches per second
e. Tape capacity of 18,000 blocks per 3600 ft. reel

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*DuPont Corporation

INPUT-OUTPUT PROCESSOR

INTRODUCTION

The Input-Output Processor (IOP) is a data processing device which controls the transfer of data between the Central Computer and Magnetic Tape Units and/or Universal Buffer-Controllers (UBC's).

During an input operation, the IOP receives data two characters at a time from the input device and assembles these characters into computer words. After each word (eight characters) has been assembled, the IOP transfers that word into the computer memory.

During an output operation, the IOP breaks down the eight-character word received from the computer memory into four groups of two characters each. As the word is processed, the IOP transfers two characters at a time to the output device.

MAJOR SECTIONS OF THE IOP (See figure IOP-1)

Functionally, the IOP can be divided into the following three major sections:

a. Connecting Matrix—establishes the electrical connections between the IOP and the I-O device.

b. Assemblers—process the data being transferred. Up to four assemblers may be contained in each IOP, and all may be operating simultaneously

c. Multiplexer—controls the operation of the assemblers.

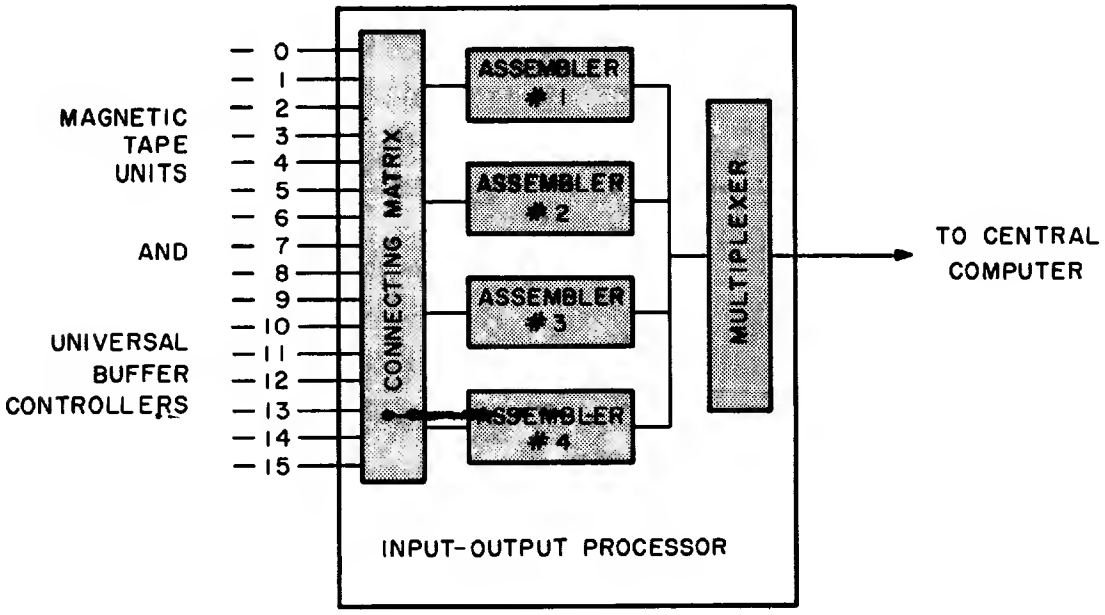


Figure IOP-1. Major Sections of IOP

To further explain the function and relationship of these sections, their basic operation is outlined in the following paragraphs, first during an input order and then during an output order.

I-O DEVICE TO MEMORY

The function of the different sections of the IOP during an input order is described below and illustrated in figure IOP-2.

a. The TIO instruction is decoded in the Central Computer and the I-O order is transferred to the multiplexer section of the IOP, where the order acceptance procedure is performed.

b. If the order can be accepted, the following actions occur:

   1. An assembler is assigned; i.e., a particular assembler is selected to process all data involved in the transmission.

   2. The connecting matrix is "marked" (electrical connection is established between the assigned assembler and the I-O device).

   3. A continue signal is transmitted to the Central Computer by the multiplexer, and transmission begins.

c. When a full word (eight characters) is assembled, the assembler signals the multiplexer, and the multiplexer makes a request to the Central Computer for memory access. Meanwhile, input transmissions continue from the I-O device.

d. The Central Computer signals the multiplexer when memory access is available, and the multiplexer allows the word to be transferred from the assembler through the IOB into memory.

MEMORY TO I-O DEVICE

The function of the different sections of the IOP during an output order is described below and illustrated in figure IOP-3.

a. Similar to input order.

b. Similar to input order.

c. After a full word, 48 bits, has been broken down into eight six-bit characters and transferred to the I-O device by the assembler, a memory request is sent to the multiplexer by the assembler.

d. The multiplexer sends a memory request to the Central Computer. When the request is granted, a new word is transferred from memory through the IOB into the assembler, and the assembler processing operations are repeated.

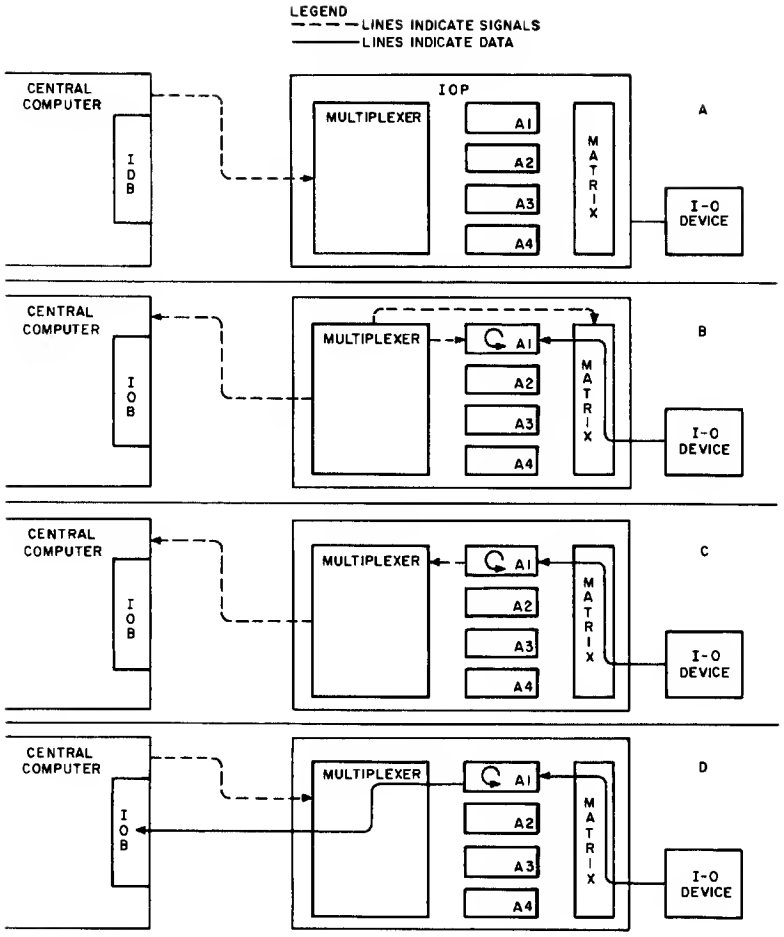


Figure IOP-2. Operation of the IOP During Input Order

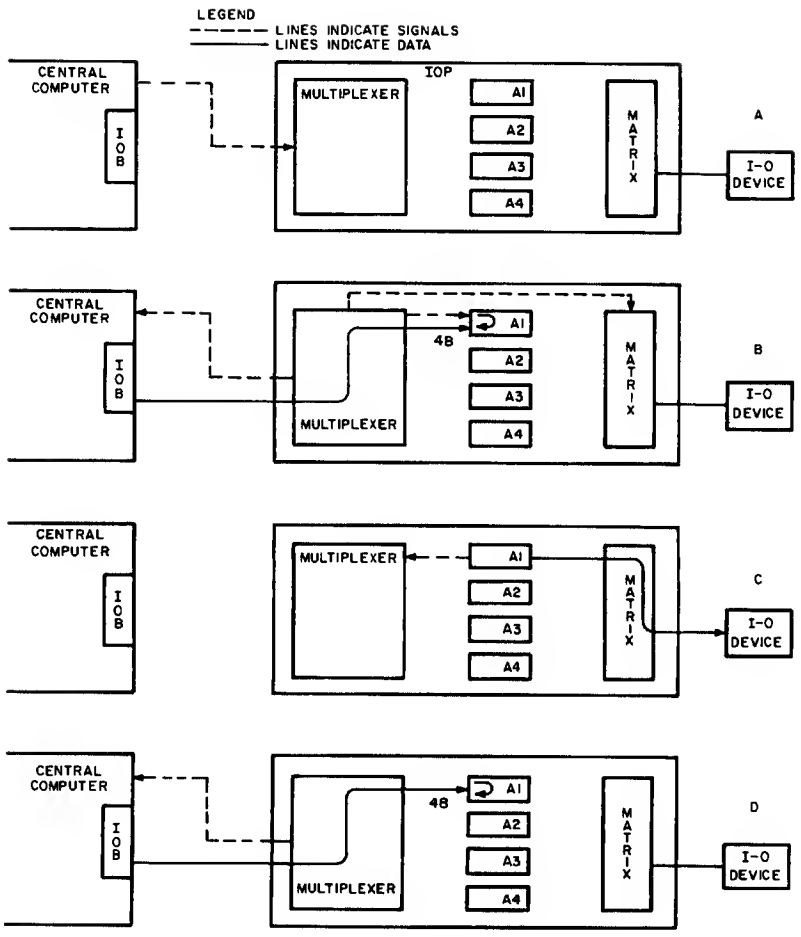


Figure IOP-3. Operation of the IOP During Output Order

DATA FLOW

In the IOP, all of the data involved in a transmission must be processed, that is, manipulated and checked. For example, in transmissions from an I-O device to memory, the input data is always received two characters at a time, processed, and then presented to the computer eight characters at a time. The reverse is true during transmissions from memory to the I-O device.

This processing is performed in the assembler, and each assembler contains various data registers which are used in the processing operation. The action of these registers, which is the same for both input and output operations, is explained in the following descriptions.

INPUT OPERATIONS (See figure IOP-4.)

In transmissions from an I-O device to memory, two characters at a time (14 bits) are transferred from the input device through the connecting matrix to a Buffer Register in the assigned assembler. In the Buffer Register each character is checked for odd parity, and the 12 data bits are transferred to the least significant bit positions of a Shift Register. The entire 14 bits are also transferred from the Buffer Register to a Write Counter, where the bits in each transfer are counted. After the last word of the block has been transferred, even channel parity is checked.

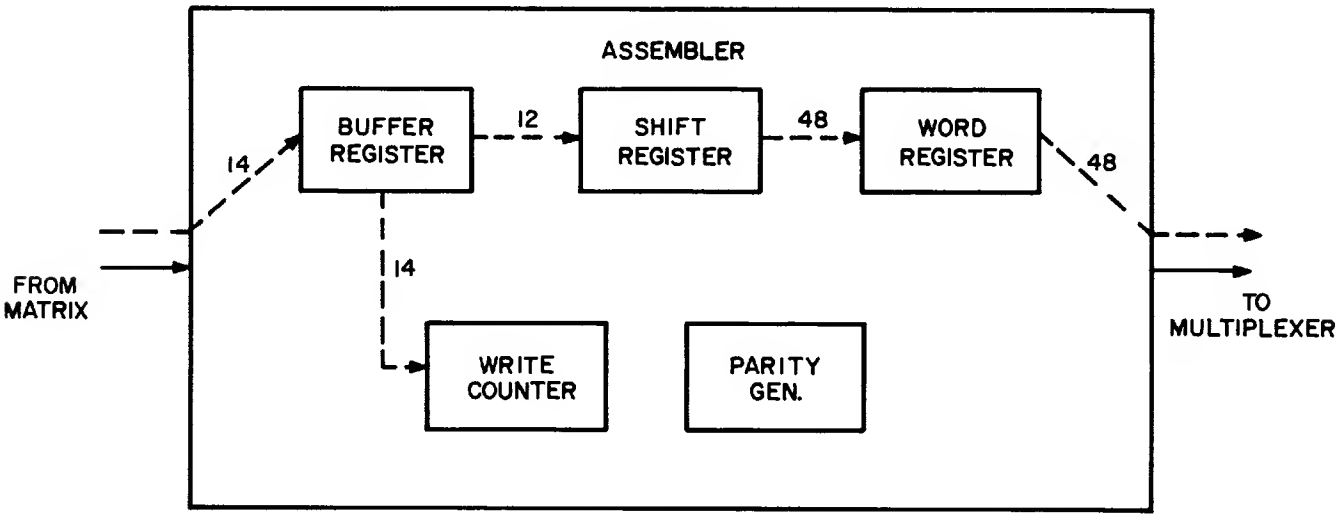


Figure IOP-4. Data Flow in Assembler During Input Order

The 12 bits placed in the Shift Register are shifted 12 places to the left to make room for the next group of 12 bits. Data is transferred from the Buffer Register until four groups of 12 bits each have been placed in the Shift Register.

When a full word is assembled in the Shift Register, its contents are transferred in parallel to a Word Register, clearing the Shift Register for the next group of 12 bits. While the word is in the Word Register, the Shift Register continues to process data and the multiplexer requests memory access. When memory access is granted, the word is transferred from the Word Register into memory.

The processing operation continues in this manner until the amount of information specified by the NO. OF BLOCKS field of the I-O order has been transferred.

When reading in the backward direction, data flow is the same as in the forward direction except that the 12 bits are transferred from the Buffer Register to the 12 most significant bits of the Shift Register. The Shift Register is then shifted to the right to assemble a word.

OUTPUT OPERATIONS (See figure IOP-5.)

In transmissions from memory to an I-O device, a full 48-bit computer word is transferred from memory through a Word Register into a Shift Register. From the Shift Register, the 12 most significant bits are transferred to the Write Counter. The Shift Register then shifts 12 places to the left so that the next 12 bits may be in position to be transferred to the Write Counter. While data is in the Write Counter, character parity bits are added by a Parity Generator. After the parity bits have been added, the Write Counter transfers the 14 bits through the connecting matrix to the output device.

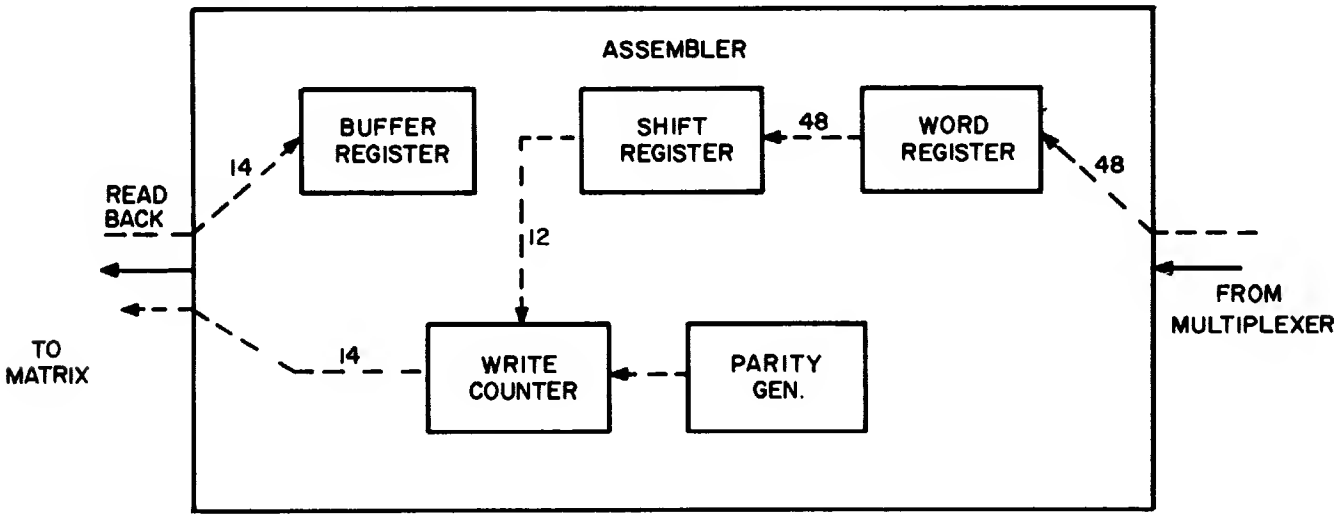


Figure IOP-5. Data Flow in Assembler During Output Order

After the data has been recorded by the output device, the recorded information is read back into the Buffer Register, where character parity is checked. The Buffer Register is then cleared, and no data is transferred to the Shift Register or to the Write Counter, since this would interfere with the writing process.

Following each transmission from the Write Counter, sprocket marks generated by the IOP are also transmitted. After a full block has been transferred, as indicated by the generation of 515 pairs of sprocket marks, the ending block mark pulses of that block are added by the IOP.

The processing operation continues in this manner until the amount of information specified by the NO. OF BLOCKS field of the I-O order has been transferred.

ACTION OF THE MULTIPLEXER

The multiplexer section of the IOP controls the selection of the particular assembler which is assigned to complete an I-O order, it also establishes access to the computer memory whenever memory is required by an assembler. When more than one assembler is operating, the multiplexer controls their sequence of transmission.

To provide the accessing function, the multiplexer monitors each assembler in sequence for a specific signal which indicates that memory is required. This monitoring action is performed continuously; however, in a four assembler system it would only require slightly more than 1 microsecond for the multiplexer to monitor all assemblers. When a signal is received from an assembler, the following operations occur, and monitoring stops until memory is accessed for that assembler.

a. The multiplexer signals the Central Computer that access is required.

b. At a time determined by the Central Computer, the multiplexer is signaled that memory is available. It is possible that more than one assembler will request memory before it can be made available; however, the request signal is maintained by the assembler, and the multiplexer executes requests in a prearranged sequence.

c. When the memory request is granted by the computer, the transfer is initiated. The Central Computer signals the multiplexer when the IOB Register contains the word being transferred.

d. The multiplexer transfers the contents of the IOB Register into the assembler Word Register during output operations, or clears the assembler Word Register during input operations.

e. In the computer, the contents of the IOB are placed into memory. During input operations, the word received from the assembler Word Register is now in memory. During output operations, the word originally in memory is restored.

IOP ACCEPTANCE OF INPUT-OUTPUT ORDERS

The IOP controls the acceptance procedure of all on-line orders issued to magnetic tape units and affects the acceptability of orders issued to intermediate-speed I-O devices connected on line to the UBC. Thus, not only must the I-O device be available before an order can be accepted, but certain conditions must also prevail in the IOP because all on-line data transmissions involving tape units and the UBC are through the IOP. The following discussion is concerned principally with the status of the IOP during the issuance of on-line orders; the conditions affecting the availability of I-O systems are described in the particular chapters dealing with these systems.

In the IOP, the acceptance of I-O orders is determined by the status of assemblers and by the contents of a certain control register, called the Unit Address Register, contained in each assembler. During data transmissions, this register contains the address of the I-O device involved in the transmission. When the transmission is completed or interrupted, the contents of the Unit Address Register are not disturbed. Instead, the address is retained until the assembler containing that register is used for another order involving a different I-O device. This fact will have significance in the discussion dealing with magnetic tape orders.

MAGNETIC TAPE AND UBC INPUT-OUTPUT ORDERS

There are 26 different magnetic tape orders and three different UBC orders. The 26 magnetic tape orders may be divided into nine different types, and the nine types, for convenience, may be subdivided into four classes; Class A, Class B, Class C, and Class D. The Class A orders include Read, Write, and Edit orders, which perform the original processing operations. The Class B orders include Stop and Release orders, which terminate processing orders and release assemblers. (The term "release" means to remove the electrical connection between an assembler and an I-O device; "terminate" means to interrupt a processing operation before it has been completed. When an order is terminated due to an error, the assembler is not released.) The Class C orders include Erase, Resume, and -1 Read orders, which provide for the resumption of processing orders which have been interrupted because of an error. The Class D orders include Rewind and Rewind with Lockout orders, which provide for rewinding tape.

There are two terms which are used to define the status of an assembler during the acceptance of I-O orders. These terms are Busy and Running, and are defined as follows:

a. Busy—indicates that the assembler is connected to an I-O device.

b. Running—indicates that the assembler is Busy and transferring data.

At the time I-O orders of each classification are executed, the status of assemblers must be as follows:

a. Class A and UBC orders—at least one assembler must be nonbusy.

b. Class B orders—the Unit Address Register of an assembler must contain the address of the I-O device specified by the I-O order.

c. Class C orders—the Unit Address Register of an assembler must contain the address of the I-O device specified by the I-O order, and that assembler cannot be running. (It is possible, using Class C orders, to cause an assembler to be reconnected to the I-O device.)

d. Class D orders—do not use assemblers.

ORDER ACCEPTANCE PROCEDURES

For the purpose of review, an I-O order which causes data to be processed through the IOP can be defined as being accepted when the contents of the D Register are transferred to the I-O system, and when the instruction which follows the TIO instruction is skipped.

Magnetic Tape Class A and UBC Orders (See figure IOP-6.)

In the acceptance procedure, the first operation determines whether or not the address of the desired I-O device is already contained in the Unit Address Register of an assembler (as a result of a previous order). The address of the I-O device is specified in the UNIT ADDRESS field of the I-O order.

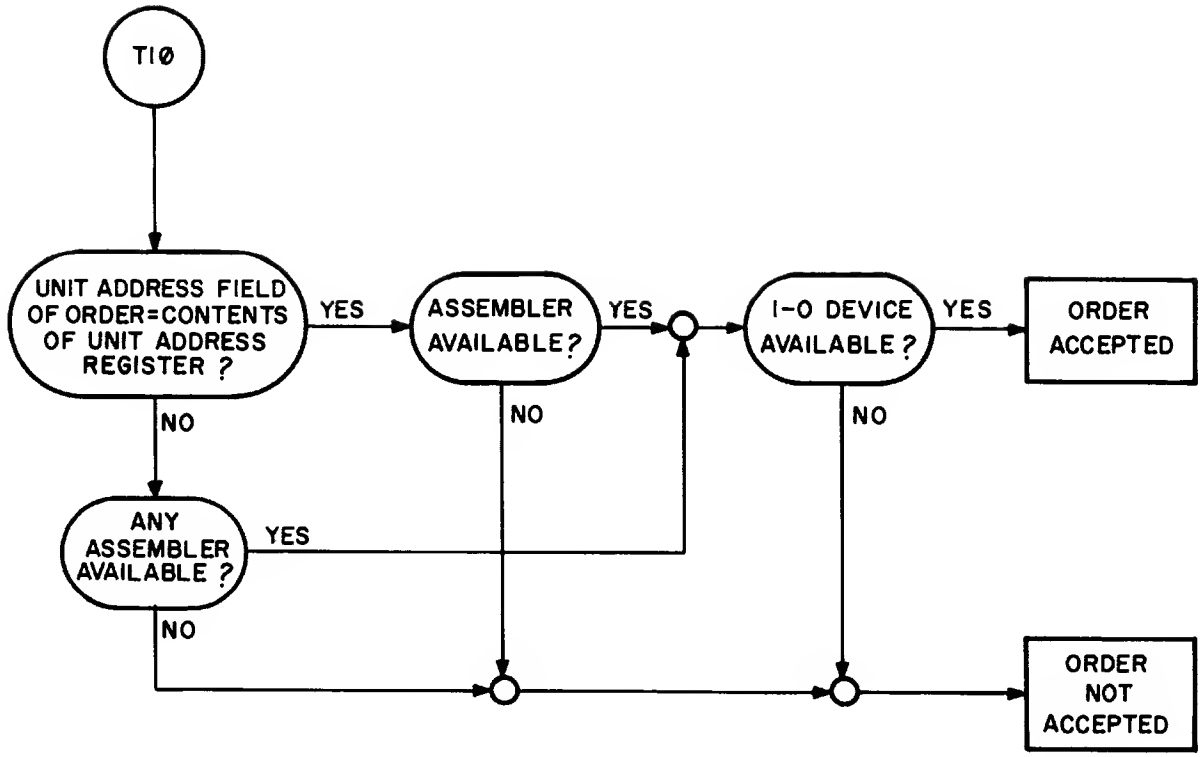


Figure IOP-6. Flowchart of Class A and UBC Order Acceptance

If the address of the desired I-O device is contained in an assembler and that assembler is nonbusy, it is selected to perform the transfer operation. If none of the assemblers contain the specified address, the lowest numbered nonbusy assembler is selected.

After an assembler has been selected, the specified I-O device is checked to determine its availability. If the I-O device is nonbusy and mechanically available, the selected assembler is assigned to the order and a "continue" signal is transmitted to the Central Computer. The continue signal indicates that the order has been accepted; the absence of the signal indicates that the order has been rejected. The Central Computer must receive the continue signal within a period of 15 microseconds after the order has been issued, or the order is treated as unacceptable by the computer.

Class B Orders (See figure IOP-7.)

In this procedure, the Unit Address Register of each assembler is interrogated. If the address specified by the I-O order is contained in an assembler, the order is accepted.

Class C Orders (See figure IOP-8.)

First, the assembler that contains the address specified by the UNIT ADDRESS field of the I-O order is selected and its run status is determined. If the assembler is in non-run status, the mechanical availability of the tape unit is checked. If the tape unit is mechanically available, the order is accepted.

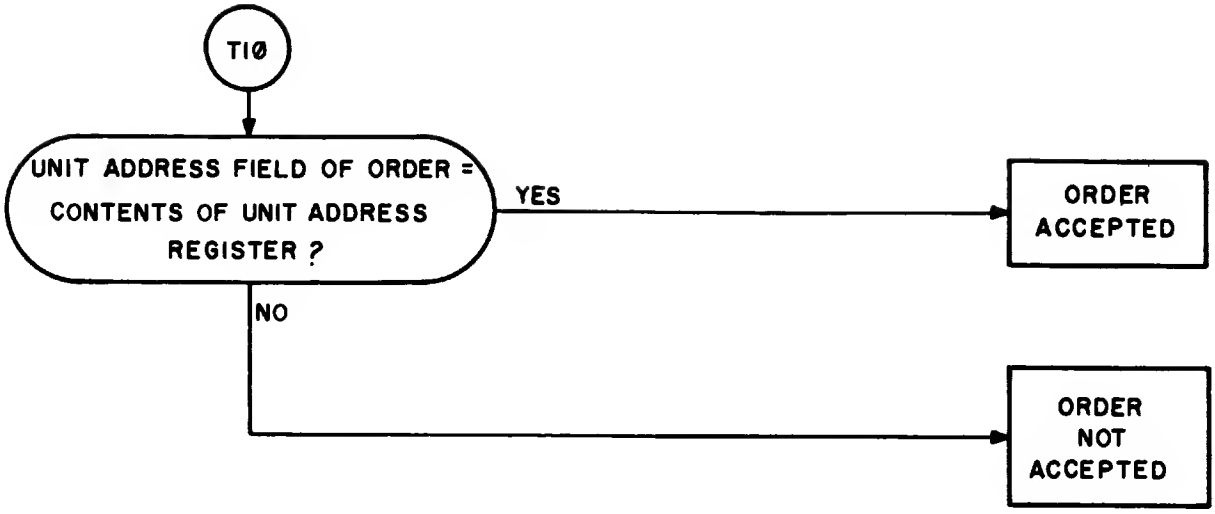


Figure IOP-7. Flowchart of Class B Magnetic Tape Order Acceptance

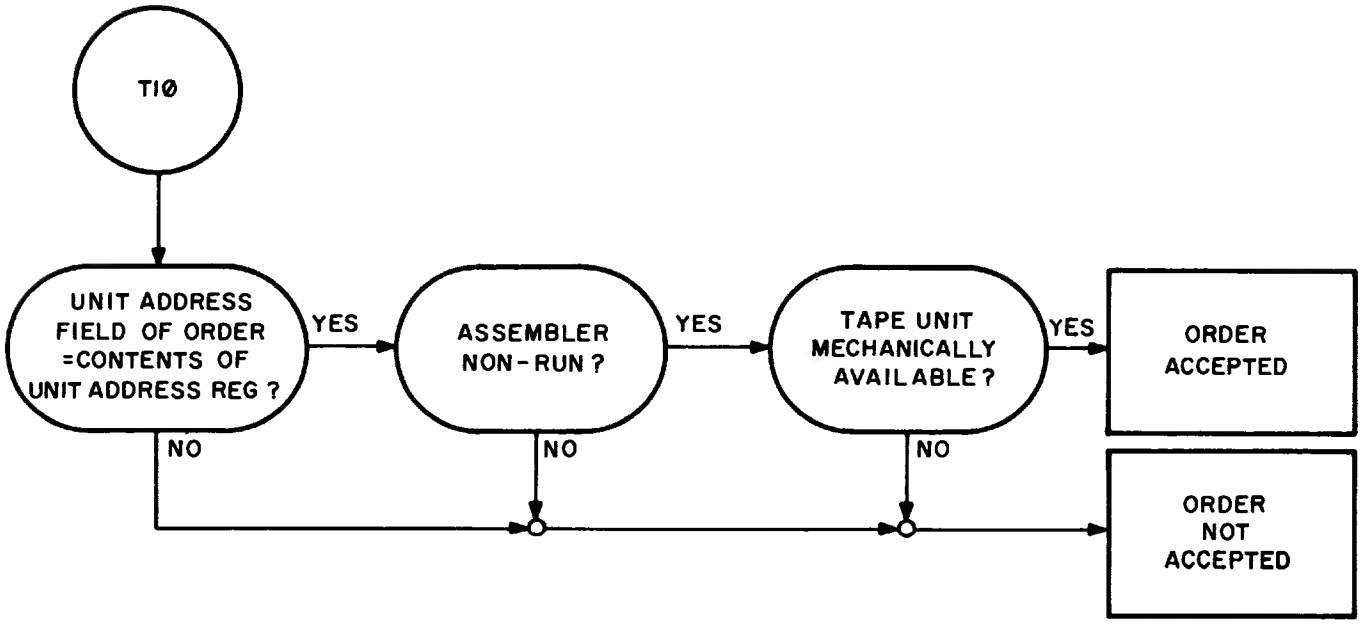


Figure IOP-8. Flowchart of Class C Magnetic Tape Order Acceptance

Class D Orders (See figure IOP-9.)

If the address of the tape unit has been correctly defined in the I-O order, and if that tape unit is mechanically available and not in run status, the order is accepted.

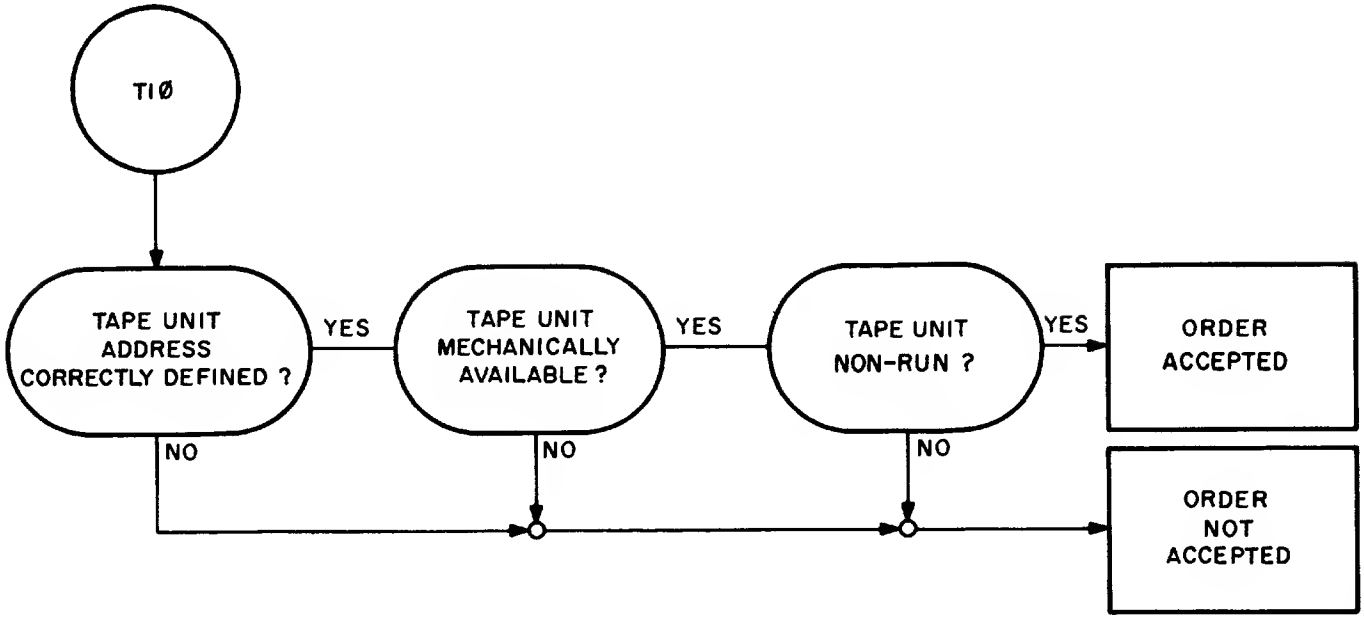


Figure IOP-9. Flowchart of Class D Magnetic Tape Order Acceptance

TRANSFER OF PARAMETERS, CLASS A MAGNETIC TAPE AND UBC ORDERS

When either a Class A magnetic tape order or a UBC order is accepted by the IOP, an assembler is assigned to the order, and control registers within that assembler are loaded with new parameters. In the case of UBC orders, only the parameter specifying the IOP CHANNEL (contained in UNIT ADDRESS field) is retained by the assembler. (The remaining parameters of the order are transferred from the D Register to the UBC.) The UNIT ADDRESS field designates the IOP channel to which the UBC is connected, and this information is used to establish the electrical connection between an assembler and the UBC.

When the I-O order is to a magnetic tape unit, all parameters of the order are transferred into appropriate control registers of the assigned assembler. Since Class B and C magnetic tape orders deal with assemblers which already have been assigned, the transfer of the parameters of these orders need not be mentioned. Therefore, only the parameters of Class A magnetic tape orders are presented in the following description.

The parameters of the I-O order are transferred from the D Register to appropriate control registers of the assigned assembler after the continue signal (indicating that the I-O order has been accepted) is received by the Central Computer. The assembler control registers and their function are as follows:

a. Command Register—receives the contents of the COMMAND field of the I-O order specifying the direction of transmission.

b. Core Storage Address Register—receives the contents of the address portion of the TIO instruction, which contains the first memory location to be accessed. The register is incremented by one each time memory is accessed.

c. Number of Blocks Processed Register—receives the contents of the NO. of BLOCKS TO BE PROCESSED field of the I-O order. The register is decremented by one each time a block is processed successfully.

d. Number of Blocks Spaced Register—receives the contents of the NO. OF BLOCKS TO BE SPACED field of the order. The register is decremented by one each time a block is spaced.

e. Unit Address Register—receives the contents of the IOP CHANNEL field of the order. This four-bit register holds the address of any one of the 16 possible IOP channels to which an I-O device may be connected.

CHECKING FEATURES

The IOP contains information registers which may be interrogated to determine the completion of an I-O order, the availability of an I-O device, and the status of an assembler. These registers are the Assembler Availability Register, the Unit Availability Register, the Assembler Counter Register, and the Assembler Fault Register.

ASSEMBLER AVAILABILITY REGISTER

The Assembler Availability Register is an eight-bit register in which each assembler is represented by two bits. One of the two bits indicates whether or not the assembler is Busy, and the other bit indicates whether or not the assembler is Running.

UNIT AVAILABILITY REGISTER

The Unit Availability Register is a four-bit register used to indicate the status of the I-O device. The conditions indicated are as follows:

a. Mechanically disabled—indicates the mechanical availability of the I-O device.

b. Running—indicates whether or not the I-O device is busy.

c. Rewinding—indicates that a tape is being rewound.

d. Read Only—indicates that the write enable ring is not mounted on the tape reel.

ASSEMBLER COUNTER REGISTER

The Assembler Counter Register contains 11 bits and displays the number of words and blocks to be processed in a Read or Write Magnetic Tape order. Four bits are used to represent the number of blocks to be processed, and seven bits are used to represent the number of words to be processed. The counter is reduced by one after each word is transferred and also by one after each block processed. Therefore, if an order were interrupted, the contents of the Assembler Counter Register would represent the number of words and blocks remaining to be processed.

ASSEMBLER FAULT REGISTER

Each assembler in the IOP contains an Assembler Fault Register, which is used to indicate transmission faults occurring between the Central Computer and the I-O device.

The Fault Register is a ten-bit register which indicates the following nine transmission errors (one bit position is not used): Space, End Tape, Begin Tape, Parity, Missing Beginning (S1) and Missing Ending (S2) Block Marks, Sprocket, Transport Disabled, and Improper Block Marks. These indications represent the following error conditions:

a. Space—results when a parity or sprocket error is detected while spacing.

b. End Tape—results when the end of a reel of magnetic tape is reached.

c. Begin Tape—results when the beginning of a reel of magnetic tape is reached during an operation other than rewind.

d. Parity—results when a character parity or channel parity error is detected.

e. S1 or S2—results when beginning or ending block marks are missing.

f. Sprocket—results when the tape is skewed or a sprocket mark is missing.

g. Transport Disabled—results when the selected I-O device goes into LOCAL while connected to an Assembler.

h. Improper Block Marks—results if the number of beginning or ending block marks pulses exceeds eight but does not total the full number of recorded block marks (16 BBM's and 17 EBM's).

OPERATING MODES OF MAGNETIC TAPE READ AND WRITE ORDERS

Magnetic Tape Read and Write orders can be issued in any one of three different operating modes. These modes, numbered 1, 2, 3, designate a particular error cycle which is followed by the IOP when a parity or sprocket error is detected during a read or write operation. (Presently, the error cycles of modes 1 and 2 are the same.)

ERROR CYCLES

The error cycles are illustrated in figure IOP-10, and are outlined as follows:

a. Read Order, Modes 1 and 2—the tape is backspaced and the block in which the error was detected is reread. If the error is present after the reread, the order is terminated at the end of the block in which the error occurred and the error indicators remain lit.

b. Read Order, Mode 3—the tape is backspaced and the block is reread. If the error is present after the reread, the error indicators are cleared and the order continues as though no error had occurred.

c. Write Order, Modes 1 and 2—the tape is backspaced and the block in which the error occurred is rewritten in the same block area. If the error is still present after the block has been rewritten, the order is terminated and error indicators remain lit.

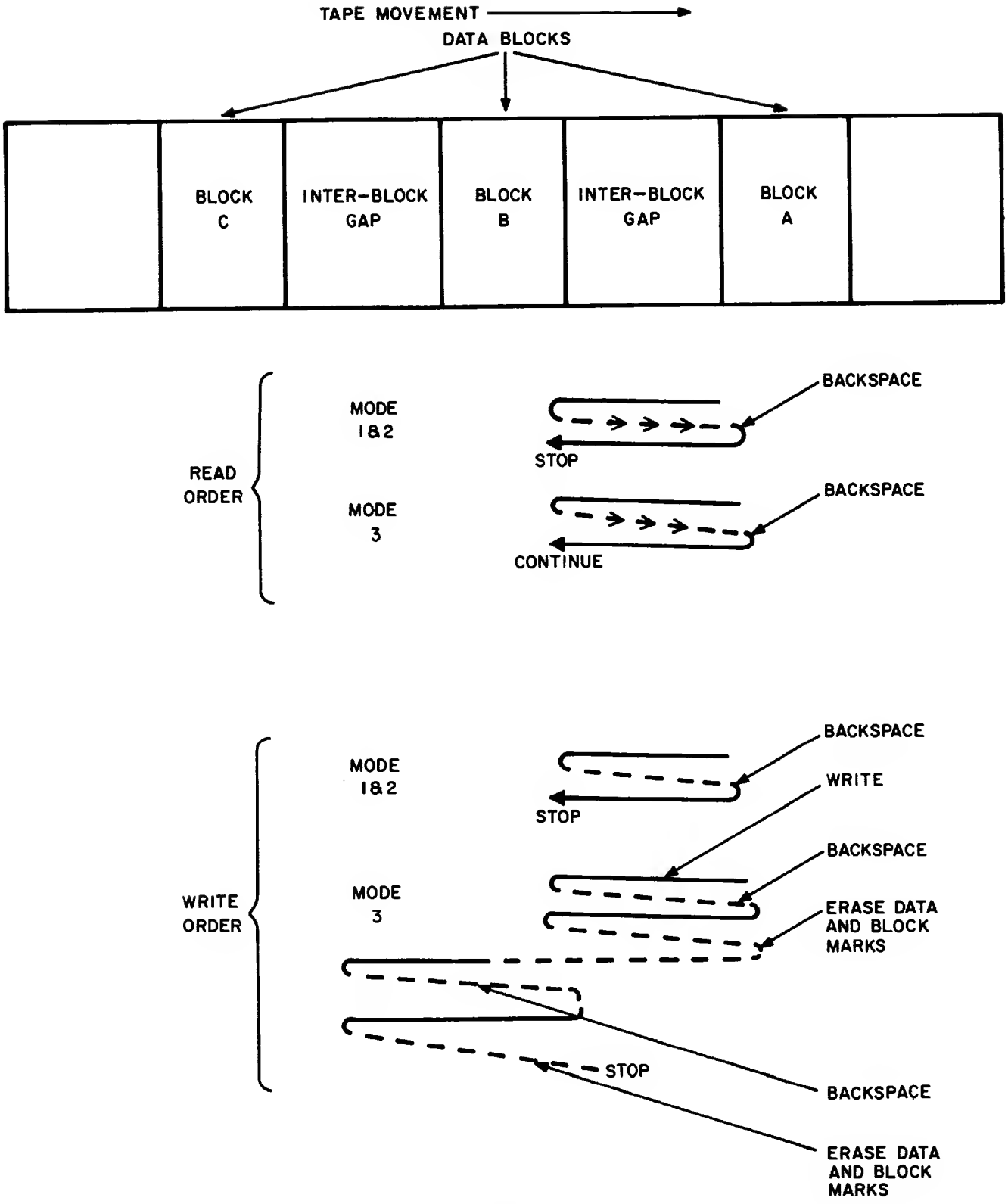


Figure IOP-10. Action of IOP Following Magnetic Tape Parity or Sprocket Errors

d. Write Order, Mode 3—the tape is backspaced and the block in which the error occurred is rewritten. If the error is present after the block has been rewritten, the block is erased and the data is rewritten in the next block area on tape. If the error is present after writing in the new area, the tape is backspaced and the block is written again. If the error is still present after this rewriting, the error indicators remain lit, the block is erased, and the order is terminated.

TAPE POSITION FOLLOWING ERROR CONDITIONS

The tape, in relation to the read/write heads of the tape transport, will not always stop in the inter-block gap following the block in which an error occurred. For example, missing ending block marks cause the tape to stop in the inter-block gap of the block following the block in which the error occurred.

To aid in determining the tape position following various error conditions, a list of the possible error conditions occurring during magnetic tape operations together with the associated tape order is presented in table 1. The table also lists the amount of information which was transferred and the contents of the assembler Word Counter Register.

The table must be used in correlation with figure IOP-11. The figure is a simplified diagram of the format of data on magnetic tape showing data block areas, beginning and ending block marks, and the inter-block gap.

To use the table, first refer to the figure and select a data block. Then, select a tape order from the table and assume any error condition from those listed in the ERROR column. In the TAPE STOP POSITION column next to the ERROR column, the position of the tape following that error condition is listed. On the diagram, locate the position listed in the TAPE STOP POSITION column to determine the position of the tape with relation to the read/write heads of the tape transport. For example, consider the following conditions:

a. Data Block A is selected.

b. The order is to read forward.

c. A parity error is detected when reading block A.

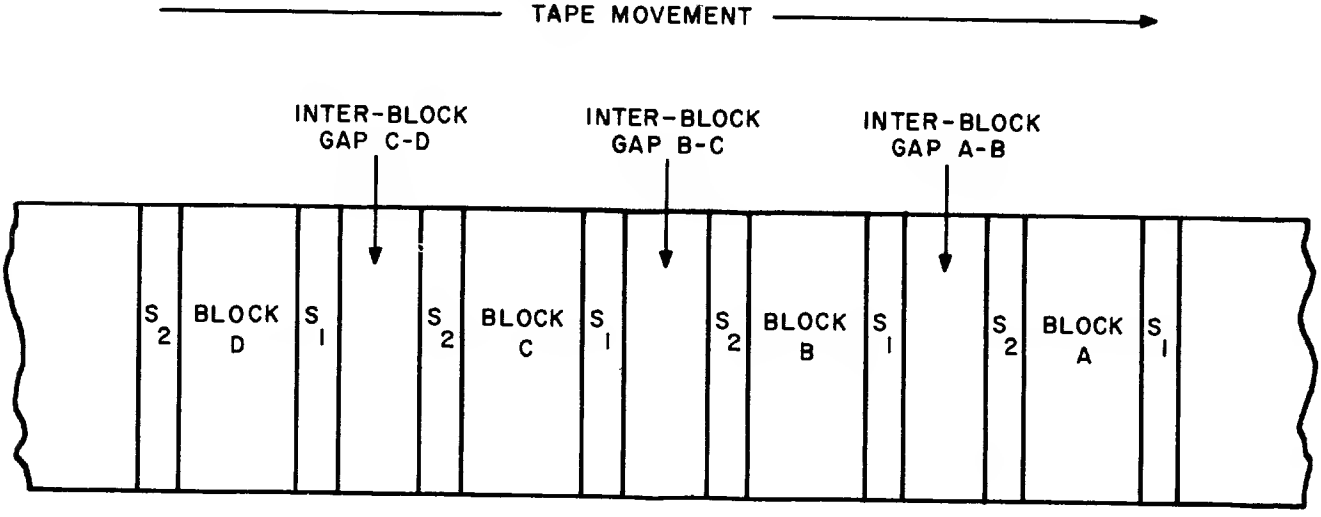


Figure IOP-11. Simplified Diagram of Block Areas on Magnetic Tape

TABLE IOP-1

TABLE OF TAPE POSITION FOLLOWING ERROR CONDITIONS

TAPE ORDER	ERROR	TAPE STOP POSITION	CONTENTS OF WORD COUNTER	INFORMATION READ
Read forward 1 block A, modes 1 and 2	Parity	A-B gap	0	Block A
	Sprocket	A-B gap	0	Block A
	Format	A-B gap	0	Block A
	S1	B-C gap	1 block	None
	S2	B-C gap	0	Block A
	Transport Disabled	Unknown	Unknown	Unknown
	End of tape	Reel stop	1 block	None
Read reverse 1 block C, modes 1 and 2	Parity	C-B gap	0	Block C
	Sprocket	C-B gap	0	Block C
	Format	C-B gap	0	Block C
	S1	B-A gap	0	Block C
	S2	B-A gap	1 block	None
	Transport Disabled	Unknown	Unknown	Unknown
	Beginning of Tape	Reel Stop	1 block	None
Write forward 1 block A, modes 1 and 2	Parity	A-B gap	0	Block A
	Sprocket	A-B gap	0	Block A
	Format	A-B gap	0	Block A
	S1	B-C gap	1 block	None
	S2	B-C gap	0	Block A
	Transport Disabled	Unknown	Unknown	Unknown
	End of tape	Reel Stop	1 block	None

From the preceding conditions, the tape would have stopped in the A-B gap; the contents of the assembler Word Counter Register would have been zero; and the contents of the data block A would have been read.

CHARACTERISTICS OF THE IOP

The operating and physical characteristics of the IOP are summarized as follows:

OPERATING CHARACTERISTICS

a. Controls up to 16 input-output channels

b. Allows four I-O devices to be operated simultaneously with the Central Computer

c. Transmission rate of 360,000 alphanumeric characters per second

d. Verifies all data transmissions

PHYSICAL CHARACTERISTICS

a. Height – 57.5"

b. Width – 118.7"

c. Depth – 18.6"

d. Weight – 2000 lbs.

UNIVERSAL-BUFFER CONTROLLER

INTRODUCTION

In the Philco 2000 Input-Output Section, the role of the Universal Buffer-Controller (UBC) is two-fold. Off-line, it provides the means to convert data from one input-output medium to another. On-line, it provides the means to couple intermediate-speed input-output devices to the Central Computer memory. When used on-line, the UBC is connected to the computer memory through the IOP.

In both functions, the UBC controls the transfer of fixed amounts of data, 128 words. In operation, it effectively matches the operating speeds of two I-O devices by receiving data at a rate compatible with the transmitting device, and then transferring that data at a rate compatible with that of the receiving device.

The transfer of a block of data, 128 words, through the UBC is always performed in two operations. The first operation, the loading cycle, is the transfer of data from its source to a one-block storage area in the UBC. The second operation, the unloading cycle, is the transfer of data from the storage area to the selected I-O device. The execution of the unloading cycle may be controlled, however, with the use of certain Philco 2000 characters.

CONTROL AND DATA SELECT CHARACTERS

The UBC recognizes two different stop characters, and, when the DATA SELECT push button on the UBC control panel is depressed, any one of 15 Data Select codes. Recognition of these control characters is a function of the UBC during off-line operations only.

The two stop characters that are recognized are the Conditional Stop (octal 52) and the Absolute Stop (octal 72). The Data Select codes are any binary representation from 1 through 15. Data Select is used to transmit only selected blocks of data to an output device. When in this mode of operation, a stop character is recognized only if it is in the selected data block.

ABSOLUTE AND CONDITIONAL STOP CHARACTERS

The UBC check the second character of the first word of each data block being loaded for an Absolute (|) or Conditional Stop (⌐) character. A Conditional Stop character is recognized only when the COND STOP push button on the UBC control panel is depressed. When either stop character is detected, transmission stops after the block containing the stop character has been unloaded to the output device.

DATA SELECT CODE

In Data Select mode, the UBC examines the last four bits of the second character of the first word of each block being loaded. If these four bits are the binary equivalent of the Data Select code (as designated by the depressed DATA SELECT push button on the UBC control panel), the block is unloaded to the designated output device. If the bits do not correspond to the Data Select code, the block is not transferred. When Data Select is not used, all data blocks are transferred in sequence.

ABSOLUTE AND CONDITIONAL STOP CODES

When the UBC is operating in Data Select mode and correspondence is found between the Data Select character of the block and the designated Data Select code, the first two bits of the character are examined for stop codes. If the first two bits are 1 and 0, a conditional stop is indicated. If the first two bits are 1 and 1, an absolute stop is indicated. A 00 and 01 in the first two bit positions have no meaning.

If an absolute stop is detected, the block is unloaded to the output device and the operation stops. When a conditional stop is detected, transmission stops after the block is unloaded only if the COND STOP push button on the UBC control panel is depressed.

ORDER ACCEPTANCE

The procedure followed by the UBC to determine the acceptance of an I-O order depends upon the type of order that is issued. That is, whether or not the order is for on-line or off-line operation.

ON-LINE ORDERS (See figure UBC-1.)

Following the execution of the TIO instruction, a series of operations initiated by the IOP is performed by the UBC to determine the acceptability of on-line orders. Before an

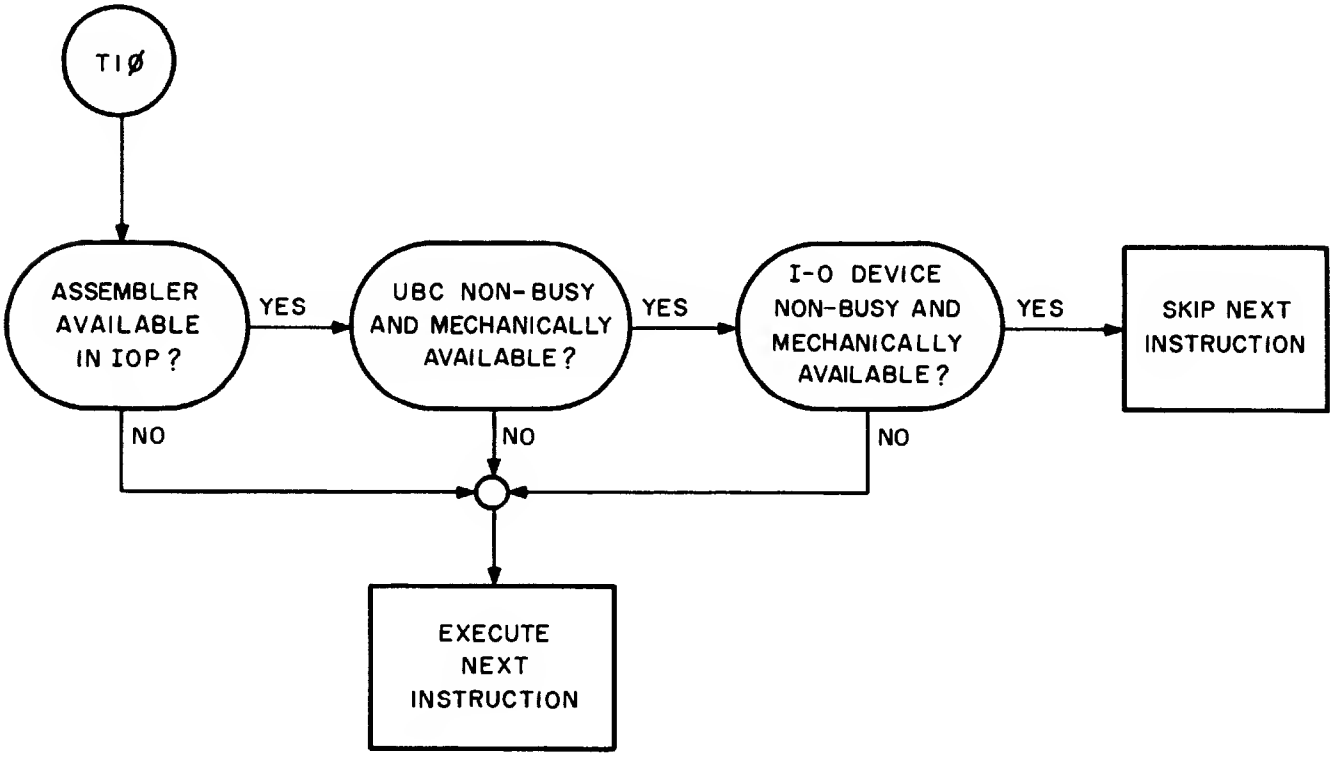


Figure UBC-1. Flowchart of On-Line UBC Order (Core to I-O Device)

order can be accepted, both the UBC and the specified I-O device must be non-busy and mechanically available. Also, the UBC must be in on-line status (the ON LINE push button on the UBC control panel must be depressed).

A Buffer Busy Register in the UBC is set whenever the UBC is busy. If this register contains a one bit, a busy condition is indicated and new orders are rejected. If the UBC is non-busy, the device specified by the BUFFER CHANNEL field of the I-O order is interrogated to determine the availability of that device.

Mechanical availability of the device is indicated by the Device Status Write and Read Available Registers in the UBC. These registers are set (contain one bits) and the appropriate indicators for each register are lit whenever an electrical connection is established between the UBC and the specified I-O device. If the device is mechanically available it is interrogated by the UBC to determine its busy status. Whenever an I-O device is busy, a Busy Register in that device is set (contains a one bit). Subsequent orders are rejected until that condition is removed, which results when the I-O device successfully completes the order in progress.

If the I-O order can be accepted by the UBC and the I-O device, the UBC transmits a "continue" signal to the IOP. The IOP, in turn, signals the Central Computer that the order has been accepted, and the next sequential instruction in the program is skipped. If the order cannot be accepted, the continue signal is not transmitted to the IOP, and the next sequential instruction in the program is executed.

OFF-LINE ORDERS

No sequential procedure is followed by the UBC during the acceptance of off-line orders, since off-line orders are initiated manually at the UBC. Off-line transmission, however, does necessitate the setting of control switches on the UBC control panel. Information describing the functions of the various controls and indicators of the UBC control panel can be found in the Philco 2000 Operating Controls Manual TM6.

MAJOR SECTIONS OF THE UBC (See figure UBC-2)

Functionally, the UBC may be divided into the following three major sections:

a. Control Section — controls the transfer of data into and out of the UBC.

b. Data Section — processes (i.e., manipulates and checks) the data as it is being transferred.

c. Storage Section — provides the temporary storage area for one block of data.

The basic function and relationship of these different sections is presented in more detail in the following description of data flow in the UBC.

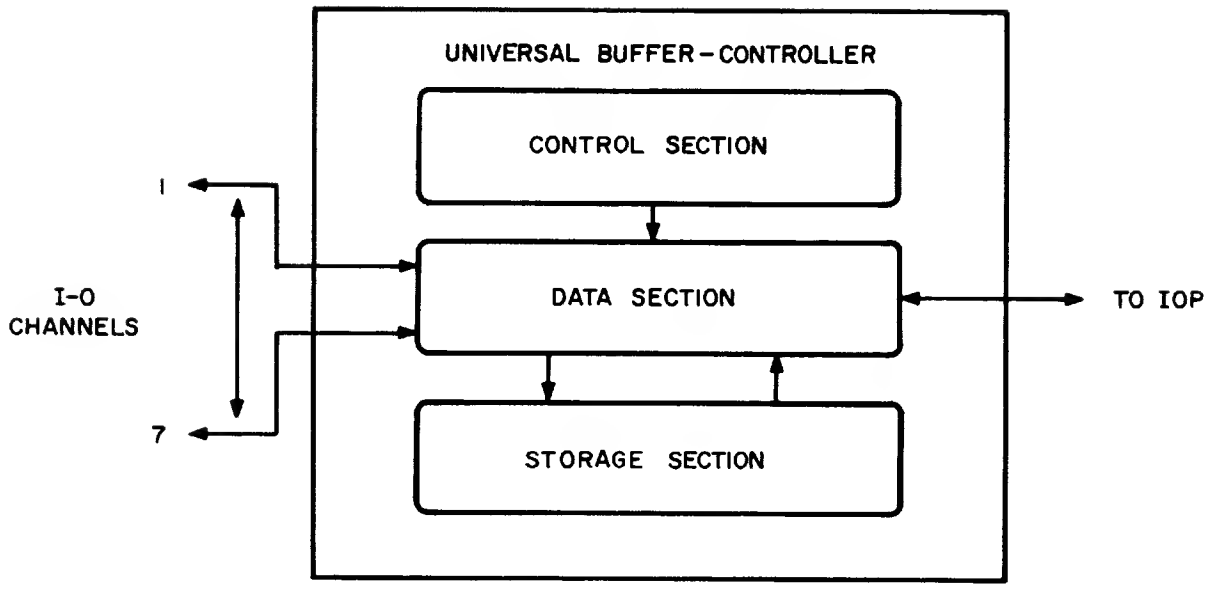


Figure UBC-2. Major Sections of the UBC

DATA FLOW

During either the loading or unloading cycles of the UBC, the format of data being transferred can be either a frame (14 bits) or a character (7 bits). Transfers of data in frame format always take place between the UBC and the following I-O devices:

a. Magnetic tape units

b. IOP

c. Punched-Card System, when Image mode is specified

d. Paper Tape System, when Image mode is specified

(The Image mode conditions of the latter two I-O systems are described in subsequent chapters dealing exclusively with these systems.)

Transfers of data in character format always takes place between the UBC and the following I-O devices:

a. Printing system

b. Punched-Card System, when Image mode is not specified

c. Paper Tape System, when Image mode is not specified

The required format of transmission is established by the UBC before a transmission begins. In operation, the UBC interrogates the transmitting and receiving devices. In the case of the Punched-Card and Paper Tape Systems, if the signal indicating Image mode is present, the UBC establishes the frame format to be used in that transmission. Otherwise, a character format transfer takes place. With magnetic tape and IOP transmissions, however, the signal indicating frame format is fixed permanently into the control wiring of the UBC channels to which these I-O devices are connected.

LOADING CYCLE DURING MAGNETIC TAPE OR IOP OPERATIONS

The loading cycle for magnetic tape or the IOP is controlled by a timing cycle in the control section of the UBC. During the loading cycle, data flow is permitted continuously from the input device into the data section of the UBC. From the data section, the data is transferred into the storage section. During the transfer into the storage section, UBC character parity is checked and if a parity error is detected, a one is placed into the appropriate bit position of the UBC fault register indicating a UBC parity error.

Data is processed in this manner until either 515 sprocket mark pairs are counted, or until the completion of the UBC timing cycle. If the timing cycle should terminate before completing its predetermined timing interval, or if 515 sprocket mark pairs are not counted before the successful completion of the timing interval, a one bit is placed into the appropriate bit position of the UBC fault register indicating a UBC edit error.

LOADING CYCLE DURING OPERATIONS INVOLVING INTERMEDIATE-SPEED DEVICES

The loading cycle for the intermediate-speed I-O devices is not controlled by a timing cycle within the UBC. Thus, the transfer is not at the continuous rate described in the IOP and magnetic tape loading cycles, but is rather, on a request basis controlled by the control section of the UBC.

This operation is initialized on a signal from the UBC called a "run reader" signal. The signal causes the reader of the specified I-O device to start operation, and as each frame or character becomes available, the I-O device transmits a "data available" signal to the UBC. On receipt of that signal by the UBC, the data is transferred from the I-O device into the data section of the UBC. From the data section, the data is transferred into the storage section and a "data received" signal is transmitted by the UBC to the I-O device. The transfer of data from the data section into the storage section is checked for character parity, and if an error is detected, a one is placed into the appropriate bit position of the UBC fault register indicating a UBC character parity error. Meanwhile, on receipt of the "data received" signal from the UBC, the I-O device makes the next data frame or character of the transmission available.

This procedure for loading data is followed until either 512 frames have been placed into the storage section, or until the number of words specified by the order has been transferred from the I-O device. If the operation calls for less than 128 words (512 frames), filler characters must be generated and transferred by the I-O device to the UBC. This procedure is required because the UBC cannot advance into an unloading cycle until the storage section is filled completely.

If the transfer is being performed off line and the UBC is not fully loaded; that is, the number of words not total 128 and filler characters are not supplied by the transmitting device, the operation will stop at the point in the loading cycle following the last character received.

In addition to character parity being checked by the UBC, parity is also checked by the I-O device. When a character parity error is detected by the I-O device, a one bit is placed in the fault register of that device. With the exception of the Punched-Card System, the UBC interrogates fault registers following the completion of each loading cycle. In the case of punched-cards, the loading cycle is interrupted immediately following the detection of an error. In all of the input systems, whenever an error condition exists it is displayed by the UBC fault register.

UNLOADING CYCLE DURING OPERATIONS INVOLVING INTERMEDIATE-SPEED DEVICES

The unloading cycle for magnetic tape and the IOP is performed in a manner similar to that of their loading cycle. That is, the operation is controlled by a timing cycle in the control section of the UBC.

Basically, UBC character parity is checked when the data is transferred from the storage section into the data section. Data is also checked for character parity when it is received by the I-O device. In the case of magnetic tape, the data is first recorded by the tape unit and then read back into the UBC, where the accuracy of the transmission is verified.

The unloading procedure is repeated until 128 words (512 data frames) have been transferred from the storage section. Again, as in the case of the loading cycle, 128 words must be transferred before the UBC can advance into the succeeding cycle.

Also included as part of the UBC unloading cycle to magnetic tape and to the IOP is the generation and transmission of sprocket marks and ending block marks. These control marks are required by both the tape units and the IOP in order to accurately record or transfer data.

During the unloading cycle, a buffer edit error, displayed by the Buffer Fault Register, may result if the UBC timing cycle should terminate before completing its predetermined timing interval, or if missing sprocket marks, or if improper or missing block marks are detected.

UNLOADING CYCLE DURING MAGNETIC TAPE AND IOP OPERATIONS

The unloading cycle to the intermediate-speed devices is similar to the loading cycle for these devices; that is, the transfer is on a request basis controlled by the control section of the UBC. This cycle is initiated by a "run punch" signal transmitted from the UBC to the designated I-O device.

Following the transmission of the "run punch" signal, the data is transferred from the storage section to the data section, and UBC character parity is checked. The data is then transferred from the data section to the I-O device. When the data is received by the I-O device, a "data received" signal is transmitted from that device to the UBC; in turn, the UBC makes the next character or frame available. This procedure is repeated until 512 frames have been transferred.

It is possible during off-line operations involving intermediate-speed devices for the UBC to stop transferring data before completing the unloading cycle. For example, if an unloading cycle to the printing system was being performed and an edit error in the printer interrupted the printing operation, a "data received" signal would not be returned to the UBC and the operation would, therefore, stop. This condition, however, could not occur during on-line operations because the UBC would assume control and complete the unloading cycle even though an error had been detected.

The conditions altering the loading and unloading cycles of the UBC during on/off-line functions are presented in more detail in later paragraphs describing the different operating modes controlling these cycles.

OPERATING MODES OF THE UBC

Effectively, the UBC is "stepped" through the loading and unloading cycles in an organized sequence of operations, called operating modes. There are eight of these modes, and of the eight, five are common to both cycles. The remaining three modes consist of two operations used only during unloading cycles and one operation used only during the loading cycle. Control passes automatically from one mode to the next as the operations of each mode are successfully completed. The sequence may, however, be interrupted if an error occurs before the loading or unloading cycle has been completed. The conditions causing variations in the operating sequence are explained in the following description, and the names given to these modes serve to indicate their functions. The modes are described as follows and are illustrated in figure UBC-3.

MODE 1, READY

The UBC must be in Mode 1 before new orders can be accepted. Actually, the UBC "idles" in this mode, and following the successful completion of an unloading cycle, the UBC returns to the Ready mode unless the CONTIN CYCLE push button on the UBC is depressed. In such a case, the Ready mode is bypassed following unloading cycles until the amount of data contained in the transmitting device has been transferred.

MODES 2 AND 3, SET UP LOADING AND SET UP UNLOADING CYCLES

The Set Up Loading and Set Up Unloading cycles cause control registers which were used during previous loading and unloading cycles to be initialized. Off line, control is passed to Mode 2 when the EXECUTE push button (located on the UBC control panel) is depressed. On line, the transfer is automatic following the acceptance of the I-O order.

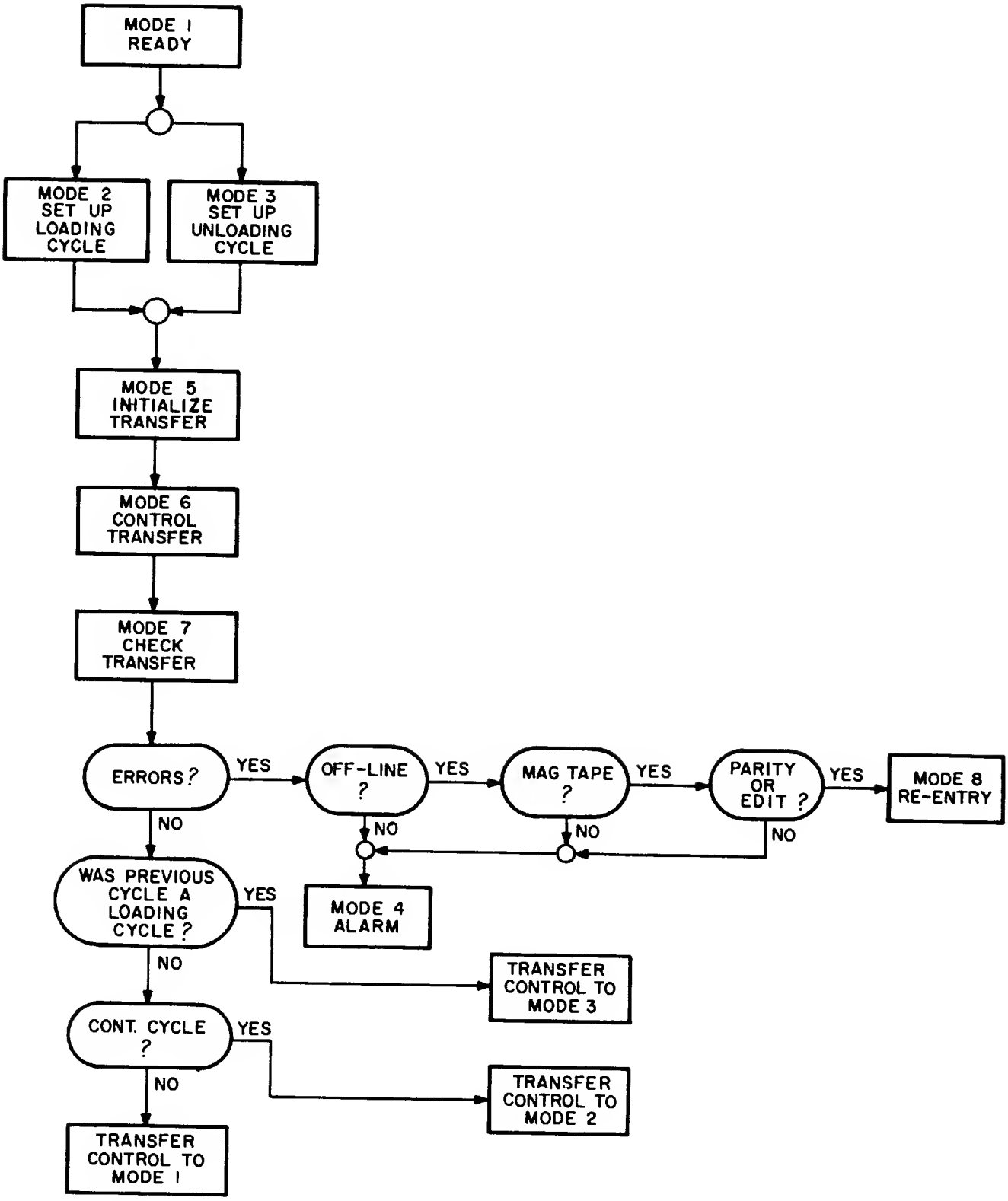


Figure UBC-3. Flowchart of UBC Operating Modes

MODE 4, ALARM

When a cycle cannot be completed successfully or when an off-line order is not acceptable, control is passed to Mode 4. In this mode, the appropriate register is set (a one bit is placed in that register) and a predetermined response to the situation is executed. The response depends upon the type of order (on-line or off-line) and the type of error that occurred. It should be noted that control can pass to Mode 4 from any of the other operating modes. If a mechanical fault occurs in either the UBC or the object I-O device, the transfer operation in all cases stops.

On line, the response to situations causing a transfer of control to Mode 4 is always to complete the order. This means entering the unloading cycle following a loading cycle, or completing the unloading cycle.

Off line, the response to most situations causing a transfer of control to Mode 4 is to stop the operation at the end of the cycle in which an error occurred. If the error is a parity error and the PARITY OVRD push button on the UBC control panel is depressed, control will pass from Mode 4 at the end of the cycle in error and return to the operation at the proper point in the sequence. That is, return will be to Mode 3 if the error occurred during a loading cycle or to Mode 1 if the error occurred during an unloading cycle. An edit error will cause the operation to stop in Mode 4.

MODE 5, INITIALIZE TRANSFER

The operations in Mode 5 cause the transfer to begin, and first data location of the storage section to be cleared.

MODE 6, CONTROL TRANSFER

All of the data transferred to and from the UBC is processed while the UBC is in Mode 6. Also included in these operations is the accessing required for each successive data location of the storage section. (Information outlining the accessing of storage locations is presented following this description of the operating modes.)

MODE 7, CHECK TRANSFER

In Mode 7, the transfer ends and the information registers of both the UBC and the I-O device are checked. Following an error-free loading cycle, the UBC enters Mode 3; following an error-free unloading cycle, the UBC returns to Mode 1. If an error is detected, the UBC enters Mode 4.

If the transfer just completed was an off-line operation involving magnetic tape, and if a beginning or ending block mark error was detected, control would pass to Mode 4 and the MAG TAPE BL MK indicator would light. If the transfer was not completed in the predetermined time period (approximately 24 milliseconds) control would pass to Mode 4 and the MAG TAPE OVRN indicator would light. If the transfer was an unloading operation and a parity or edit error was detected, control would pass automatically to Mode 8.

MODE 8, RE-ENTRY

Mode 8 is entered during off-line unloading operations to magnetic tape in which a parity or edit error occurs. This mode allows another transfer (one re-entry) of the same block to be attempted automatically.

BUFFER STORAGE ACCESSING

Data locations in the buffer storage section are accessed in a fixed sequence of locations, and this accessing is performed while the UBC is in Mode 6. Each location in the storage area is frame size (14 bits) and, regardless of the established transmission format (7 or 14 bits), data is read into and out of the storage area frame-at-a-time. During character-at-a-time loading cycles, the characters are assembled and loaded frame-at-a-time. During character-at-a-time unloading cycles, the storage area is unloaded frame-at-a-time, but the data is transferred to the receiving device character-at-a-time.

In the loading cycle the sequence is write and then read. The write operation places data into a storage location, and the read operation clears the next sequential storage location.

In the unloading cycle the sequence is read and then write. Then read operation removes data from a storage location, and the write operation restores that data to the same location. Restoration allows a re-entry (a reattempt at unloading a block) to be executed.

CHECKING FEATURES

The status of the UBC is indicated by a five-bit Buffer Fault Register in the UBC. Parity and edit errors which may occur in either the I-O device or the UBC, and mechanical faults which may occur in the I-O device are represented by this register. The I-O error conditions that are indicated by the Buffer Fault Register are covered in subsequent chapters describing each I-O device; the UBC error conditions that are indicated have already been discussed.

CHARACTERISTICS OF THE UBC

The operating and physical characteristics of the UBC are summarized as follows:

OPERATING CHARACTERISTICS

a. Storage capacity of 1024 characters (128 words)
b. Seven separate I-O channels
c. Off-line data conversions between any two Philco 2000 input-output media
d. Verification of all data transmissions
e. Simultaneous operation of four UBC's on line

PHYSICAL CHARACTERISTICS

a. Height — 57.5"
b. Width — 61.2"
c. Depth — 18.6"
d. Weight — 1000 lbs.

PUNCHED-CARD SYSTEM

INTRODUCTION

The Punched-Card System provides the Philco 2000 computer with a means of accepting input from punched-cards and of recording output on punched-cards. The card system consists of a high-speed photoelectric card reader, a card punch, and a card controller. As shown in figure PC-1, both the reader and the punch are connected to the controller, and the controller is connected to the UBC. This arrangement permits transmission of data to and from the Punched-Card System either on line with the Central Computer or off line with other input-output devices.

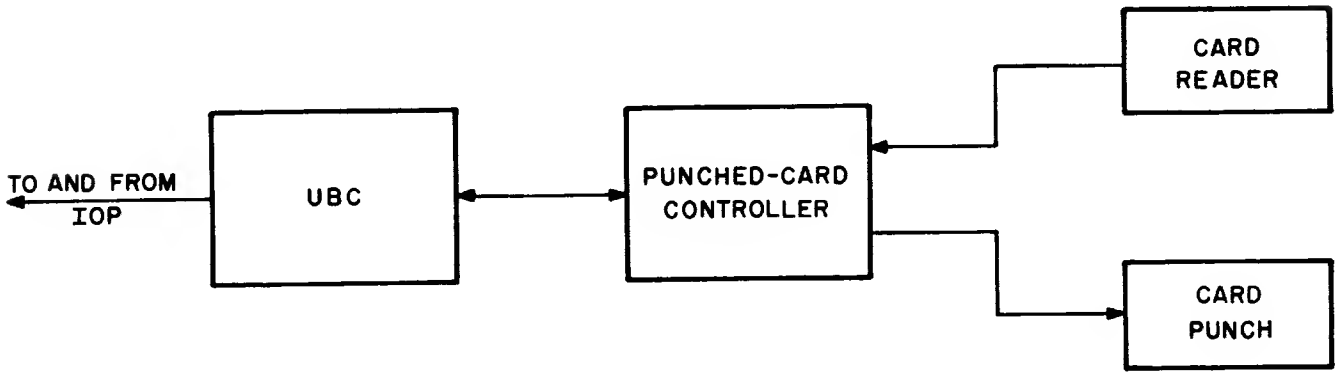


Figure PC-1. Tie-In of Punched-Card System with 2000 System

CARD FORMAT

As illustrated in figure PC-2, a card is divided vertically into 80 columns and horizontally into 12 rows. Each column contains 12 bit positions and each row contains 80 bit positions. Reading or punching of cards is performed a row at a time: when reading, row 9 is processed first; when punching, row 12 is processed first.

DATA FORMAT

Data may be processed on cards in either Philco 2000 code or in Hollerith code. In Hollerith code, one character is represented in each column; in Philco 2000 code, two characters are represented in each column. The first character of the Philco code is represented in rows 12, 11, 0, 1, 2, and 3, and the second character is represented in rows 4

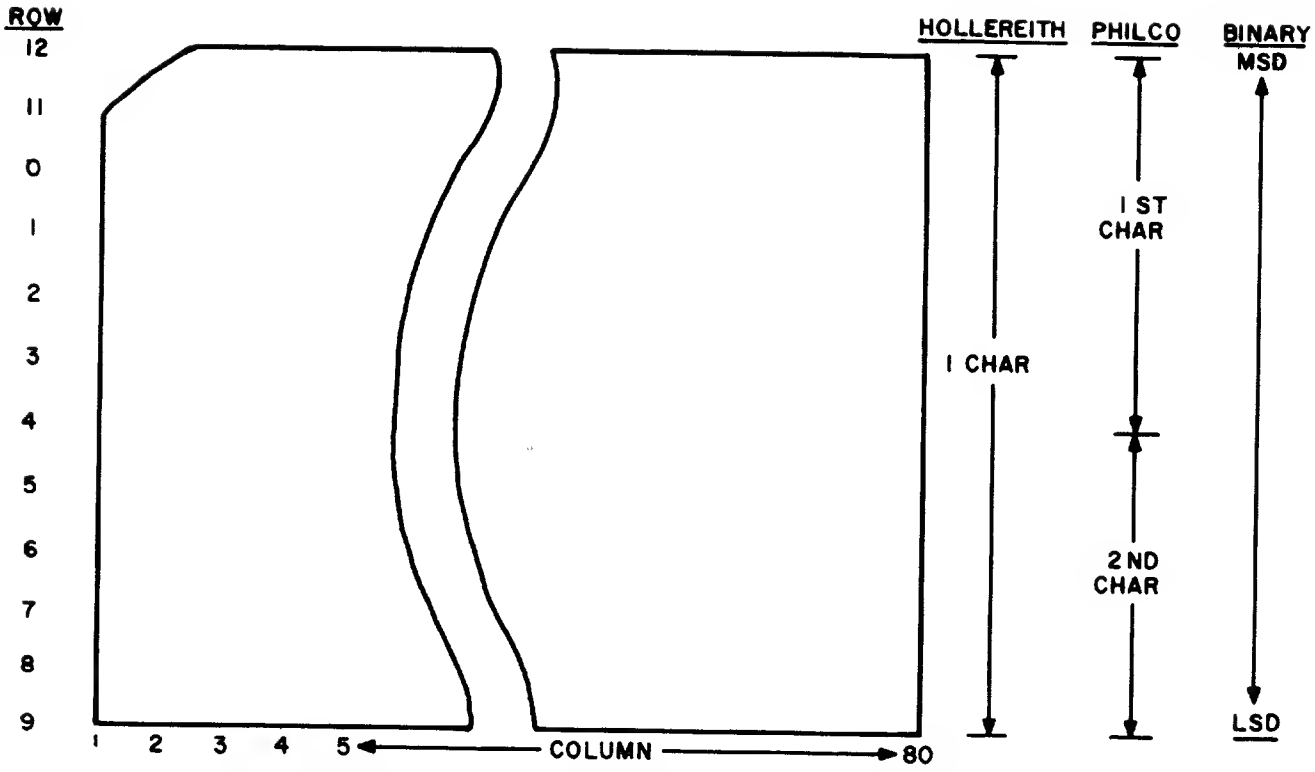


Figure PC-2. Punched-Card Format

through 9. The Punched-Card System makes no distinction between binary numbers and Philco 2000 characters. Binary numbers recorded in a column have the most significant digit (MSD) recorded in row 12, and the least significant digit (LSD) recorded in row 9.

The position of a CODE/IMAGE switch on the control panel of the card controller determines the code which is used in the processing operation. When the switch is set to IMAGE, Philco code interpretation is effected; when the switch is set to CODE, a Hollerith code interpretation is effected.

FORMAT CONTROL

The format in which data is read from cards or punched on cards is determined by control characters and by two control registers in the card controller, called the Word Register and the Card Register. The Word Register specifies the number of words to be contained on one card, and the Card Register specifies the number of cards to be contained in one block. On line, these registers receive their information from the AMOUNT OF INFORMATION TO BE TRANSMITTED field of the I-O order; off line, they receive their information from plugboards. (More information concerning the function of plugboards is given later in this chapter.)

RELATION OF WORDS/CARD AND CARDS/BLOCK

During processing operations, the Word Register is decremented by one each time a word is either punched or read. When the Word Register equals zero, it indicates that the end of a card has been reached. The Card Register is decremented by one each time a card is either read or punched. When the Card Register equals zero, it indicates that the end of the block has been reached. Each time the Card Register is decremented, the contents of the Word Register are restored.

CONTROL CHARACTERS

Three control characters are used by the Punched-Card System: the end-of-block, the end-of-card, and filler characters. A CNTRL CHARS switch on the panel of the card controller provides the option of either sensing or ignoring these characters.

End-of-Card Character

The end-of-card character (octal 77) within a word causes it to be the last word punched on, or read from a card, even though the Word Register may call for more words. When punching, if the end-of-card character is not the last character of a word, all characters subsequent to that character must be filler characters, or an edit error results. When reading, the card controller generates filler characters to fulfill the requirement.

End-of-Block Character

The end-of-block character (octal 52) has all of the effects of an end-of-card character, and in addition, causes the present card to be the last one processed in the block, even though the Card Register may call for more cards. When punching, all characters subsequent to the end-of-block character must be filler characters, or an edit error results. When reading, the card controller generates filler characters until 128 words have been transferred.

Filler Character

The filler character (octal 32) is used to fill out words and blocks in order to satisfy the requirements of a minimum of one word/card and 128 words/block. These characters may appear between any two non-control characters. When the filler character is sensed during the punching operation, it is not punched, but is replaced by the character that follows it. During the reading operation, the filler character is treated as if it were a data character; that is, it is counted and transferred to the UBC.

It should be noted that during punching operations, recognition of filler characters at the end of blocks or after end-of-card characters does not depend upon the position of the CNTRL CHARS switch. When such recognition is necessary but does not occur, an edit error results.

THE PUNCHED-CARD CONTROLLER

The Punched-Card Controller assembles, checks, and stores information transmitted to it until all of the information contained on one card has been stored. It then transfers that information to either the UBC or to the card punch, depending upon the operation being performed (reading or punching).

Functionally, the card controller consists of five principal sections; the control section, the translator, the card buffer, and read and punch plugboards. (See figure PC-3.) In the controller, the necessary control functions are performed. These functions include, for example, controlling the data format (words/card and cards/block), generating parity bits and filler characters when reading, and checking row parity when punching.

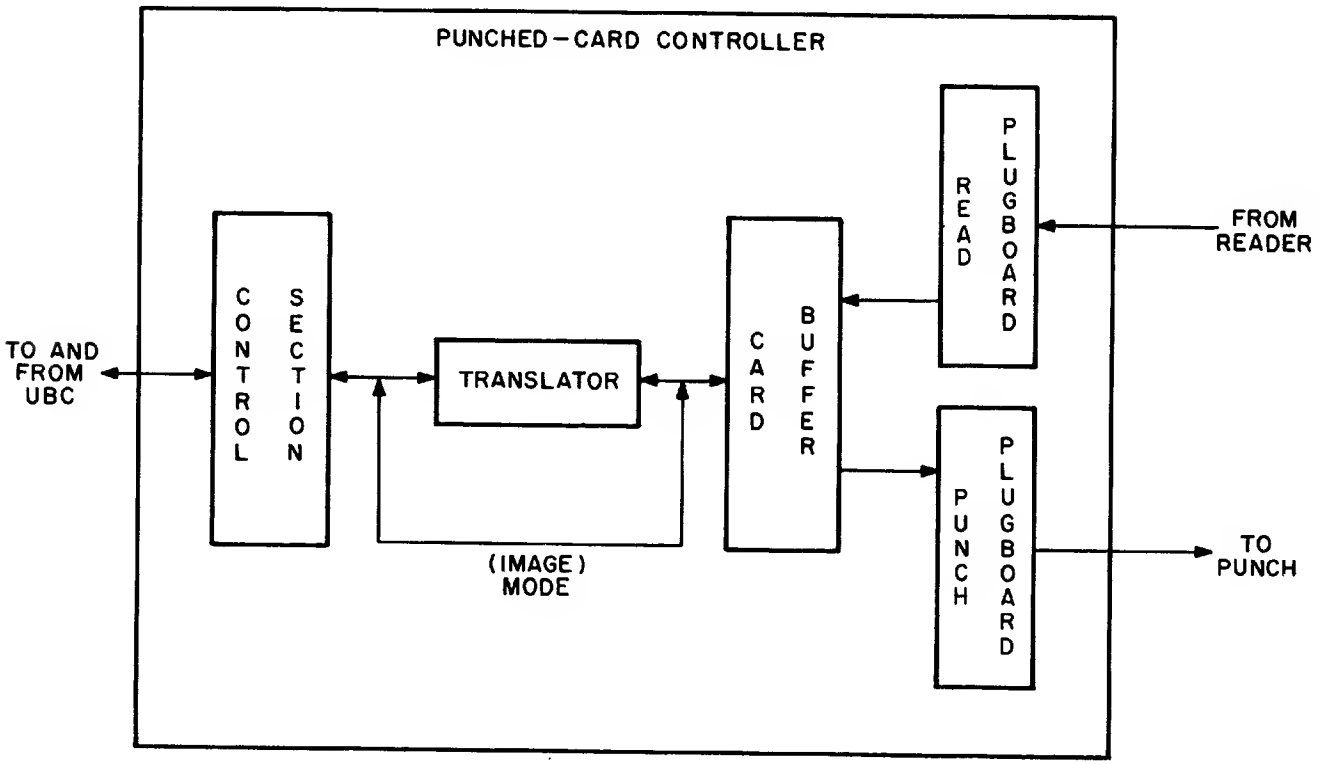


Figure PC-3. Principal Components of Punched-Card Controller

Data transferred between the UBC and the control section is always in Philco code, which may be either 14 bits (frame) or 7 bits (character) at a time. Data transferred between the control section and the card reader or punch, however, may be in either Philco or Hollerith code. The translator is located between the control section and the card reader and punch. When required, the translator may be used to convert data into or from Hollerith code. This conversion takes place only when the card system is operated in Code mode; in Image mode the translator is bypassed.

Storage in the card controller is provided by a card buffer, which has the storage capacity of one complete card. With Philco characters, this capacity would be a maximum of 20 words/card (80 columns ÷ 4 columns/word = 20 words/card). With Hollerith characters, this capacity would be a maximum of 10 words/card (80 columns ÷ 8 columns/word = 10 words/card). The card buffer is used to facilitate conversions between data transmitted by rows from the reader or to the punch, and data transmitted by columns to and from the UBC.

Transmission of data to the punch and from the reader is via plugboards. The punch plugboard allows data to be punched in a different columnar pattern than that which was received from the UBC. Likewise, columns read may be rearranged at the read plugboard before being sent to the UBC. Furthermore, up to eight columns of fixed data may be substituted at the plugboards for data received from the UBC to be punched, or for data read from cards to be sent to the UBC.

During off-line operation, the plugboards control the number of words that are to be punched on each card and the number of cards that will contain one block of data.

There is one plugboard for the reader and one for the punch, and they are not interchangeable. Information is manually wired into these plugboards.

ACCEPTANCE OF PUNCHED-CARD ORDERS

The acceptance of on/off line orders issued to the Punched-Card System is determined by the UBC, and the acceptance procedure is described in detail in the chapter dealing with the UBC.

ACCEPT EX CARD CONTROL

The ACCEPT EX CARD control, located on the card controller, is meaningful only when control characters are being used to control a reading operation. With this method of control, the end-of-block character is not interpreted until that character is transferred from the card buffer to the UBC. Before the decision to stop the operation can be made, however, the next sequential card will have been read by the reader and placed in the card buffer. Therefore, in order to save the contents of the card following the card which contains the end-of-block character, the ACCEPT EX CARD push button must be depressed. When depressed, this control causes the contents of the card buffer to be read as the first card of a block at the start of a reading operation.

CHECKING FEATURES

The Punched-Card System checks for parity, edit, and mechanical faults during the performance of a punched-card operation. These faults are indicated on the control panel of the Punched-Card Controller.

PARITY FAULT INDICATIONS

Punched-card parity faults are indicated by the PARITY error indicator on the control panel of the card controller, and the following conditions cause that indicator to light:

a. when an unrecognizable Hollerith code is detected during a reading operation in Code mode

b. when there is an even number of bits (including the parity bit) in one row during a punching operation.

If a parity error is detected and the OVERRIDE PARITY push button is depressed, the operation continues until all processing is completed. If a parity error is detected and the OVERRIDE PARITY push button is not depressed, the PARITY error indicator lights and the operation is interrupted at that point. If the parity error occurs during a punching operation, the card which contains the error is notched in columns 67 through 72.

EDIT FAULT INDICATION

Punched-card edit faults are indicated by the EDIT ERROR indicator on the control panel of the card controller, and the following conditions cause that indicator to light:

a. when 128 columns have been transmitted and the end of the card has not been indicated either by the end-of-card character or by the Word Register equalling zero

b. when 128 words have been transmitted and the end of the block has not been indicated either by the end-of-block character or by the contents of the Card Register equalling zero

c. when less than 128 words have been transmitted and non-filler characters are detected following the end of block character

When an EDIT ERROR is detected during a punching operation, processing continues until one block, 128 words, has been transferred. When reading, the operation is interrupted at the point where the error is detected.

MECHANICAL FAULT INDICATIONS

Mechanical faults in the Punched-Card System are indicated by the MECHANICAL FAULT READER and PUNCH indicators on the card controller. They are caused by the following conditions:

a. the photoelectric reading mechanism is not functioning properly

b. the cards are jammed in the card reader

c. the internal timing of the reader is faulty

d. the card being read is skewed

e. the card hopper (the container which holds the cards before they are processed) is empty

f. the card stacker (the container which holds the cards after they have been processed) is full

g. a plugboard is missing or is inserted incorrectly

When any of the mechanical fault indications are present, the operation stops at the point where the error is detected and the card system remains electronically connected to the UBC. In the case of the skew fault, however, the operation does not stop if the OVERRIDE SKEW push button on the card controller is depressed. In the case of the fault indications caused by the card hopper being empty, the card stacker being full, or a card being skewed, the operation may be continued from the point at which it was interrupted by the fault. In all other causes of mechanical faults, the operation should be restarted from the beginning.

CHARACTERISTICS OF THE PUNCHED-CARD SYSTEM

The operating characteristics of the Punched-Card System are summarized as follows:

a. Punching rate of 100 cards per minute

b. Reading rate of 2000 cards per minute

c. Hopper capacity - 4000 cards (reader), 700 cards (punch)

d. Checking of parity, card alignment, and system components

e. Codes recognized - reads and punches Hollerith and card Image mode

f. Automatic card counter

PAPER TAPE SYSTEMS

INTRODUCTION

Two different paper tape systems are available for use with the Philco 2000. One system, Model 240, is operated over the Word-At-A-Time Channel and is connected directly to the IOB; the other system, Model 241, is operated through the UBC. These systems permit the 2000 computer to accept input data from paper tape and to record output data onto paper tape. In general, both systems may be used on line, and both may be used to read or punch five- and seven-level paper tapes. There are, however, additional features of the Model 241, which include off-line applications, and the capacity for reading and punching eight-level tape.

Both systems consist of a high-speed photoelectric Paper Tape Reader, a Paper Tape Punch, and a Paper Tape Controller. The reader and the punch are connected to the controller, and the controller is connected to either the IOB or to the UBC, depending upon the system being considered.

DATA FORMAT (See figure PT-1)

The format of data on paper tape can be either five-, six-, seven-, or eight-bit code combinations, which are recorded on tapes of five, seven, and eight channels (levels). Five-bit codes are recorded on five-channel tape; six- and seven-bit codes are recorded on seven-channel tape; eight-bit codes are recorded on eight-channel tape.

Data of any format is recorded on paper tape in frames across the width of the tape. As each frame is recorded, sprocket holes are punched, which provide a means of movement while the tape is being punched and a means of detecting data areas while the tape is being read. In each frame, data is always recorded with three bits of the code combination on one side of the sprocket hole and the remaining number of bits on the other side.

In the Model 240 System, the five-bit code is treated as a six-bit character, with a zero in the most significant bit position. With Model 241, however, five-bit codes are treated as a six-bit character by adding a one bit in the most significant bit position. An exception to this procedure is explained in the discussion of the Model 241 System presented later in this section.

The six-bit code consists of one six-bit character without a parity bit and is recorded on seven-level tape.

The seven-bit code consists of one six-bit character and a parity bit. The value of this bit is chosen to make the total number of one-bits in the frame odd. During the recording process, the parity bit is recorded with the character and occupies channel seven of the tape.

In eight-bit codes, each frame is treated as two six-bit characters by adding zeros to the four most significant bit positions of the first character formed. The first character is comprised of four zeros and the data from channels 7 and 8 of the tape. The second character is comprised of the data in channels 1 through 6 of the tape.

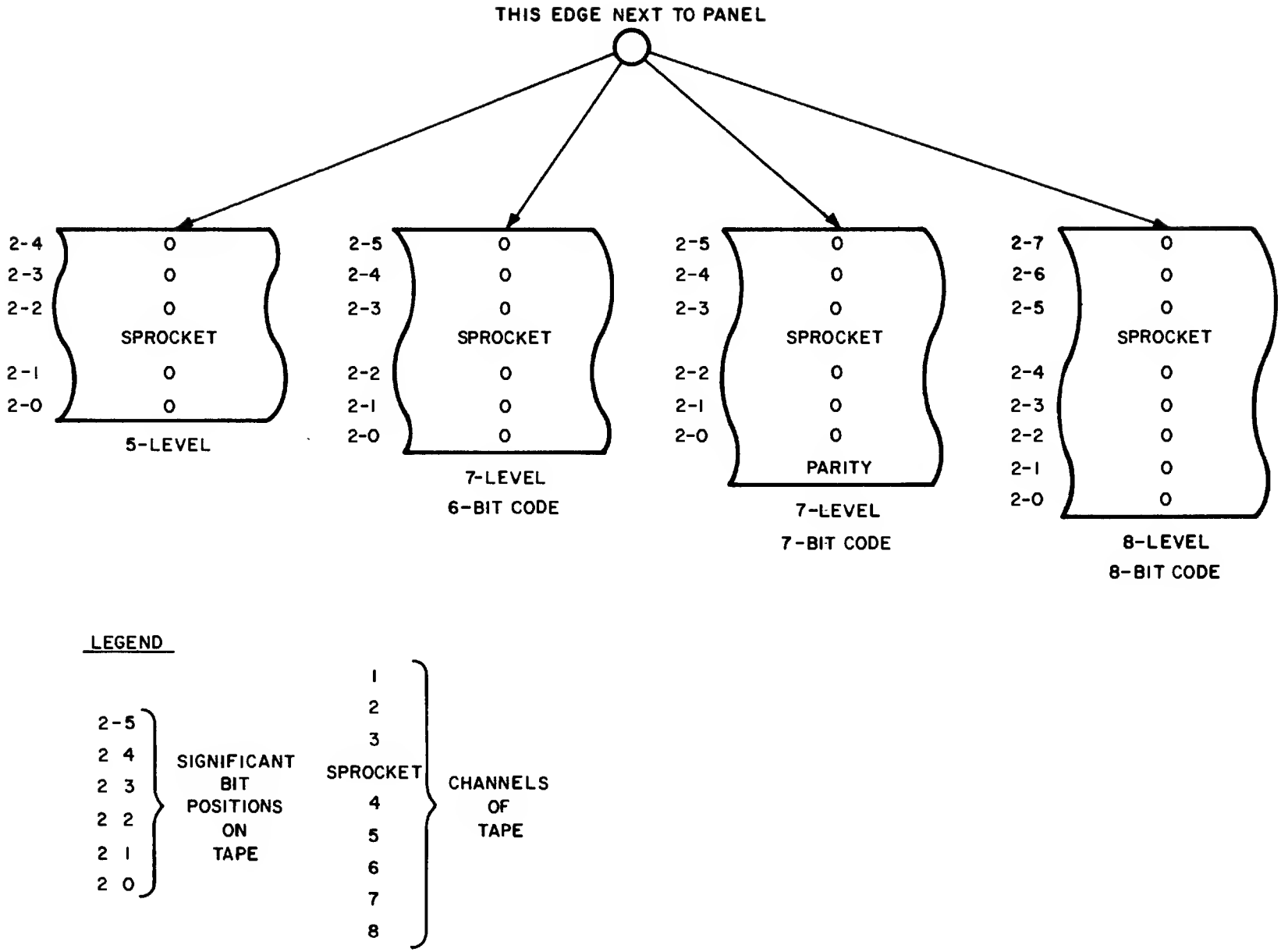


Figure PT-1. Data Format on Paper Tape

PAPER TAPE SYSTEM, MODEL 240

The Paper Tape System, Model 240, is operated with the Central Computer over the Word-At-A-Time Channel. The system receives data from and transmits data to the Central Computer memory through the IOB. All transmissions, therefore, are one full computer word (48 bits), and all are on line.

In Philco 2000 installations which make use of an Accounting Clock System, the Clock is coupled to the computer memory through the controller of this system. Figure PT-2 is a simplified block diagram showing the tie-in of the major components of the Paper Tape System, including the Clock.

I-O ORDER ACCEPTANCE, MODEL 240 (See figure PT-3.)

The Paper Tape System must be both mechanically available and non-busy before an I-O order can be accepted. When the system is busy, a Busy Register in the tape controller is set, and subsequent orders are rejected until that register is reset. The Busy Register is reset after the number of words specified by the I-O order have been transferred, and during reading operations, when a stop character is recognized.

CONTROL CHARACTERS

The Stop character, octal 72 (represented by the symbol "|"), is the only control character used by the Model 240 System. This character has effect only during the reading operation, and, when recognized, releases the tape system from an input-output order regardless of whether or not the number of words specified by that order have been read.

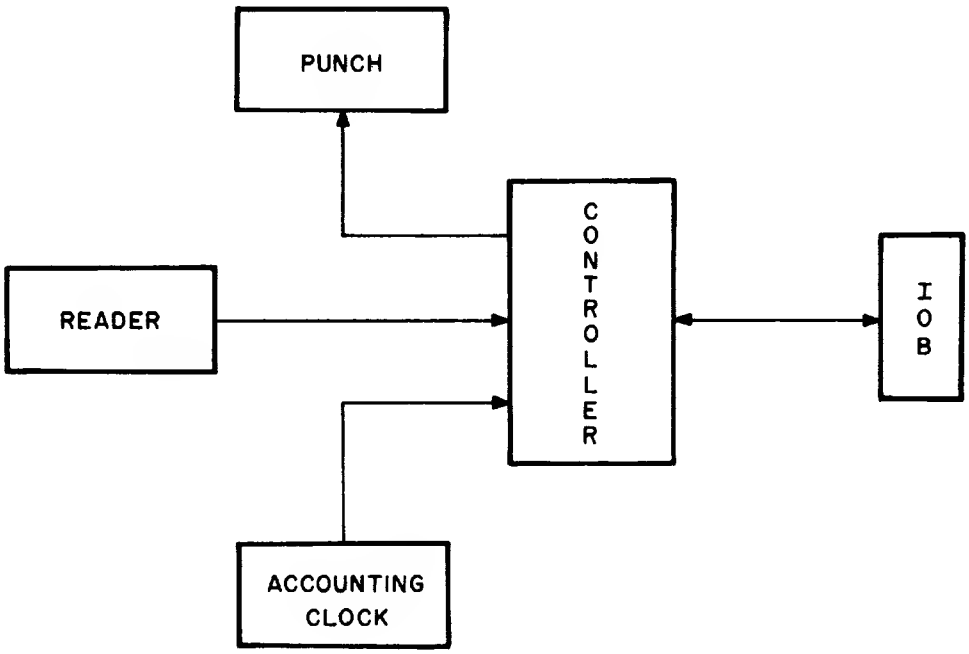


Figure PT-2. Tie-In of Major Components of Paper Tape System, Model 240, Simplified Block Diagram

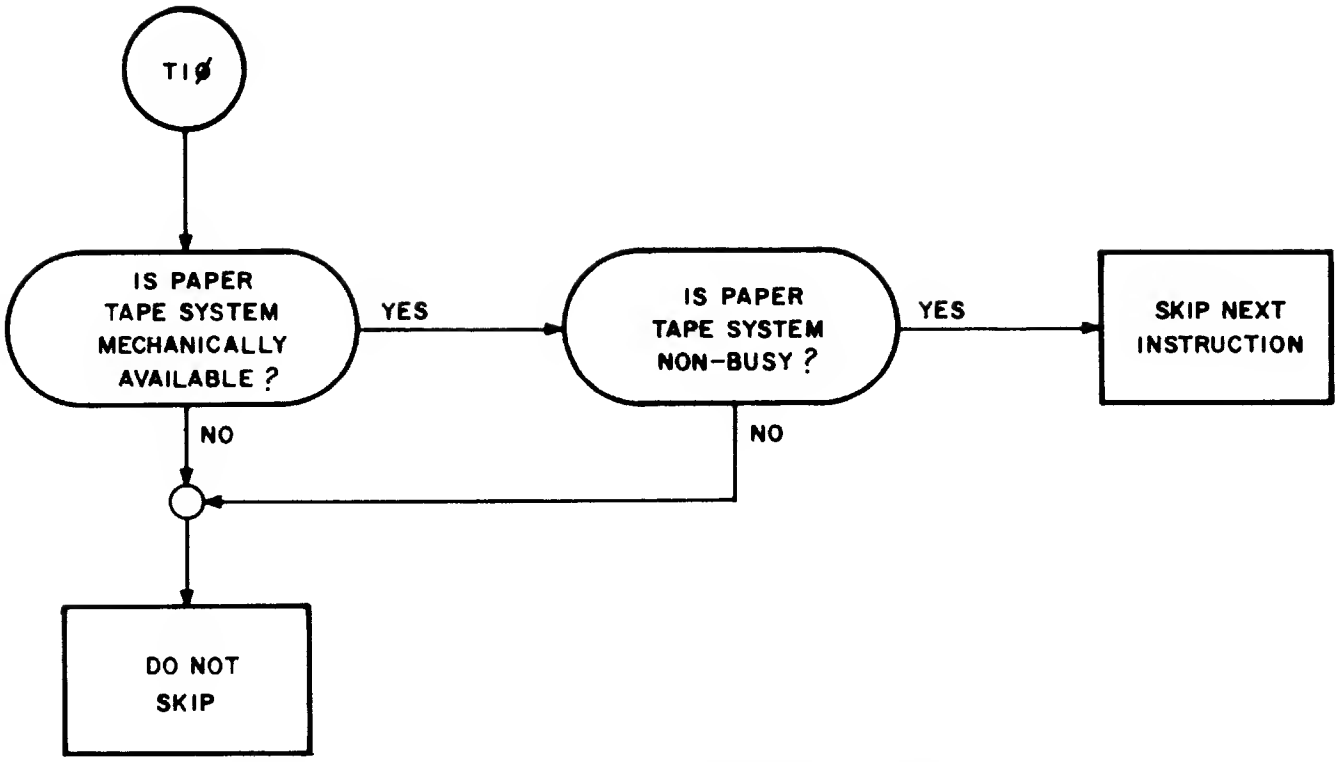


Figure PT-3. Flowchart of Paper Tape System, Model 240, Order Acceptance Procedure

Stop character recognition is controlled by the use of a STOP CHAR. BY PASS switch located on the control panel of the Paper Tape Controller. The switch has two positions, ON and OFF. In the OFF position, stop characters will be recognized and will control the operation; in the ON position they are bypassed.

DATA FLOW, MODEL 240

The processing operations of the Paper Tape System, other than the actual reading or punching of data, are performed by data and control registers of the Paper Tape Controller. The functions of these registers are presented in the following description of data flow during processing operations.

DATA FLOW DURING THE READING OPERATION (See figure PT-4.)

During a reading operation, the Paper Tape Reader transfers one frame (character) at a time to a Paper Buffer Register in the tape controller. If the frame is a blank (i. e., no punches other than a sprocket hole), the next frame is read from the tape automatically. In the Paper Buffer Register, each character is examined for the presence of a stop character, and if seven-bit codes are being read, the character is also checked for odd character parity and the parity bit is deleted.

After each character is examined, it is moved from the Paper Buffer Register into the six least significant bit positions of a 48-bit Paper Word Register, also in the tape controller.

As each character is entered into the Paper Word Register, the contents of the register are shifted six positions to the left to allow the next character to be entered. When either eight characters or a stop character has been transferred from the reader into the Word Register, the contents of the Word Register are transferred through the IOB into the computer memory, and the Word Register is cleared. After the eight characters have been transferred into memory, a Word Counter Register (located in the tape controller) is decremented by one. If after being decremented by one the Word Counter equals zero, the operation stops and the Busy Register in the tape controller is reset. If the Word Counter does not equal zero, processing continues until either the Word Counter equals zero, or a stop character is sensed.

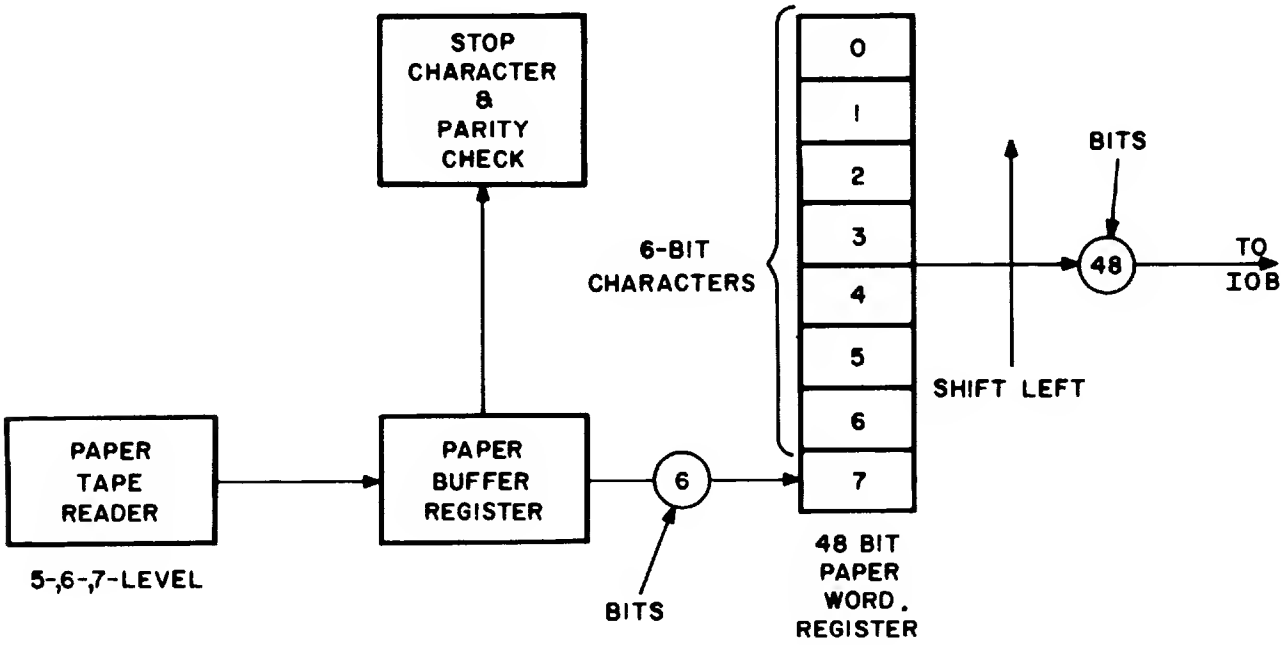


Figure PT-4. Data Flow During Paper Tape System, Model 240, Reading Operation

DATA FLOW DURING THE PUNCHING OPERATION (See figure PT-5.)

During the punching operation, a full computer word (48 bits) is transferred from the computer memory through the IOB into a 48-bit Word Register in the tape controller. The six most significant bits of the computer word are then transferred from the Word Register into a Paper Buffer Register, and the contents of the Word Register are shifted six positions to the left to make the next six most significant bits available for transfer. From the Paper Buffer Register, the six bits are transferred to the Paper Tape Punch, where they are recorded and a sprocket hole is punched. If seven-bit code is being recorded, a parity bit is added to the six data bits while that character is in the Paper Buffer Register.

The next six most significant bits of the Word Register are transferred to the Paper Buffer Register and the processing cycle is repeated. Processing continues in this manner until eight characters (one word) have been transferred from the Word Register to the punch.

After a full word has been punched, a Word Counter (in the tape controller) is decremented by one. If the Word Counter does not equal zero after being decreased, the next word is transferred from the computer memory into the Word Register, and the first character of that word is processed. When the Word Counter equals zero, the punching operation stops and the Paper Tape System is released from its busy status.

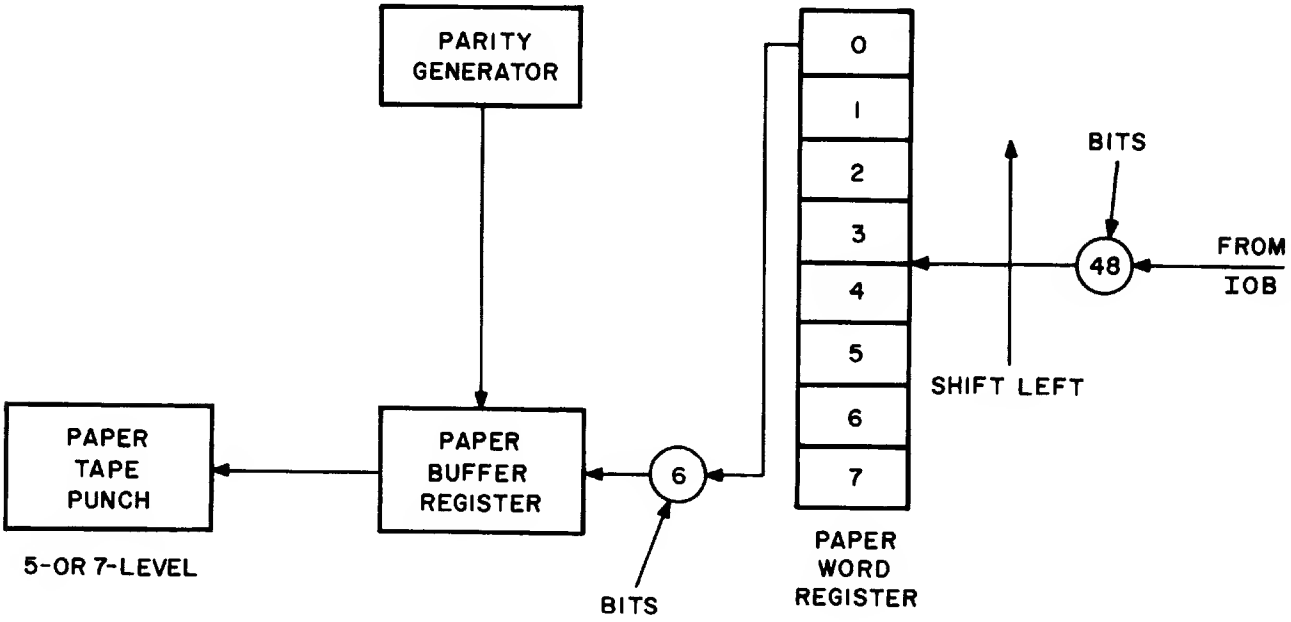


Figure PT-5. Data Flow During Paper Tape System, Model 240, Punching Operation

OPERATING CONTROLS, MODEL 240

Control switches on the control panel of the Paper Tape Controller provide the option of either recognizing or ignoring stop characters and parity errors occuring during paper tape operations. These controls are the PARITY ERROR (STOP and BY PASS) and the STOP CHAR. BY PASS (ON and OFF) switches.

Parity Error Switch

If a character parity error is detected when reading seven-bit code and the PARITY ERROR switch is set to STOP, the order is terminated and the contents of the Word Register are not transferred to memory. The character which contains the error is the last character transferred from the Paper Buffer Register into the Word Register; if reading is continued, that character will be transferred to memory. If a character parity error is detected when reading and the PARITY ERROR switch is set to BY PASS, the error is ignored and the operation continues. (Parity is not checked during a punching operation since the value of the parity bit is determined while the six-bit character is in the Paper Buffer Register.)

STOP CHAR. Switch

If a stop character is detected during the reading operation and the STOP CHAR. BY PASS switch is set to OFF, the six bits that represent the stop character are transferred from the Paper Buffer Register to the Word Register, and the contents of the Word Register are read into memory. The operation then stops and the Paper Tape System is released from its busy status. If the stop character is detected and the STOP CHAR. BY PASS switch is set to ON, the stop character is ignored and the operation continues.

If the stop character did not occur at the end of a word, all characters following the stop character of the word would be transmitted as zeros. For example, if the stop character were the fourth character of a word and if the first three characters of the word were A, B, and C, the eight characters transmitted to memory, in the order of their significant bit positions would be as follows: 00000ABC.

CHECKING FEATURES, MODEL 240

The Paper Tape Controller contains two registers which may be interrogated to determine the status of the Paper Tape System and to determine whether or not an error occurred during a transfer of data through the system. These registers are the Paper Tape Transmission and the Paper Tape Fault Registers, and their functions are as follows:

a. Paper Tape Transmission Register — a two-bit register used to indicate the status of the Paper Tape System. One bit in the register indicates whether or not the tape system is busy, and the other bit indicates whether or not the designated number of words have been transmitted (Word Counter Register equal or not equal to zero).

b. Paper Tape Fault Register — a one-bit register used to indicate when a character parity error has been detected.

THE ACCOUNTING CLOCK SYSTEM

The Accounting Clock System (Clock) is an optional feature available with the Philco 2000 computer, and is used on line to transmit the date (month and day) and the time of day (hour, minute, and tenth of minute) to memory. In operation, the Clock automatically corrects the date for the length of months (30 and 31 days). A switch is provided to correct for the 28 or 29 days of February. Switches also allow for initial Clock setting.

THE ACCOUNTING CLOCK WORD

The date and time form a Clock word which is 36 bits in length; 16 bits represent the date and 20 bits represent the time of day. All quantities are represented in four-bit binary coded decimal characters. Of the four characters representing the date, two BCD characters represent the month, and two BCD characters represent the day. Of the five characters representing the time of day, two BCD characters represent the hour, two BCD characters represent the minute, and one BCD character represents the tenth of minute. As shown in figure PT-6, a Clockword occupies the 36 least significant bits of the 48-bit Philco 2000 word; the 12 most significant bits are all zeros.

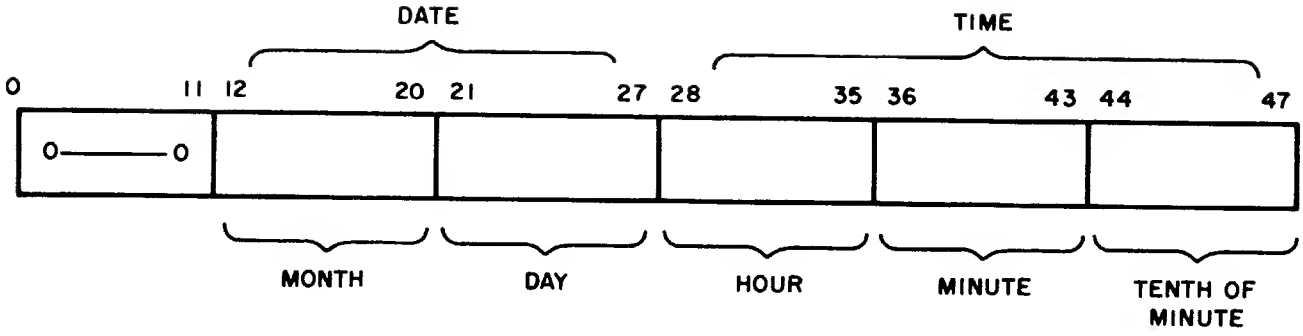


Figure PT-6. Format of Accounting Clock Word

SYSTEM TIE-IN

The Accounting Clock System is used on line and is addressed by a Paper Tape I-O order. The Clock shares access to the Central Computer memory with the Paper Tape System, Model 240. Since the command code of the input-output order is the same for both the Clock and Paper Tape System, a one or zero in location 20 of the UNIT field of the I-O order is used to specify whether the Clock or the Paper Tape System is desired. A one designates that the Clock is being addressed, and a zero designates that the Paper Tape System is being addressed. The parameters of the input-output order for the Clock are shown in figure PT-7.

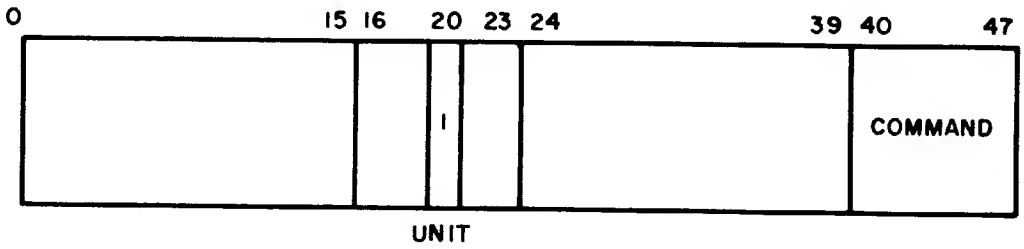


Figure PT-7. Accounting Clock System Input-Output Order

ORDER ACCEPTANCE, ACCOUNTING CLOCK SYSTEM

The acceptance of a Clock order is determined by the paper tape controller, and the order is not accepted if either the paper tape or Clock systems are busy, or the Clock system is mechanically disabled. If the Clock is changing time when the order is accepted, the contents of the Clock will be transferred to memory at the completion of the time change. A flow chart outlining the action of the Clock order is illustrated in figure PT-8.

CHECKING FEATURES

The two-bit Transmission Register of the Paper Tape System is used to determine wheth-whether or not the transfer of the Clock word has been completed. (The register is checked by the Skip Check instruction for the Paper Tape System.)

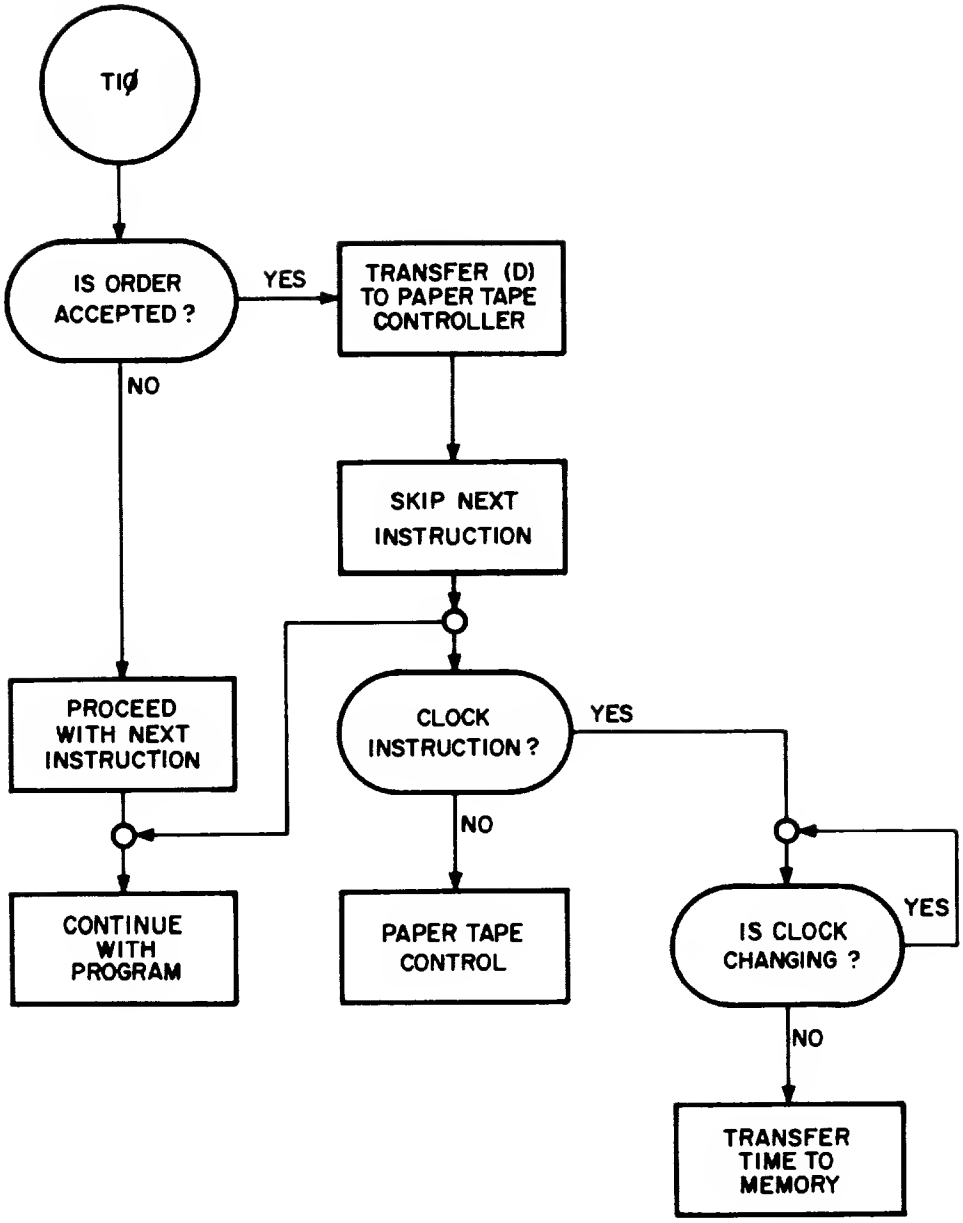


Figure PT-8. Flowchart Outlining Action of Clock Order

The first, or interlock, bit of the register indicates completion of the Clock order. If the interlock bit is zero, the word has been transferred; if the interlock bit is one, the word has not been transferred. The second bit, or Word Counter, of the register is meaningless to the Clock, since only one word will be transferred, regardless of the setting of the bit in the counter.

PAPER TAPE SYSTEM, MODEL 241

The Paper Tape System, Model 241, is designed to be operated through the Universal Buffer-Controller of the Philco 2000 System. Since all operations are performed through the UBC, the tape system may be operated either on or off line, and may process up to a maximum of 128 words per input-output order.

The Paper Tape System consists of a high-speed photoelectric Paper Tape Reader, a Paper Tape Punch, and a Paper Tape Controller. Both the reader and the punch are connected to the controller, and the controller is connected to a channel of the UBC. A simplified block diagram of the Paper Tape System showing the tie-in of the system with the Central Computer is illustrated in figure PT-9.

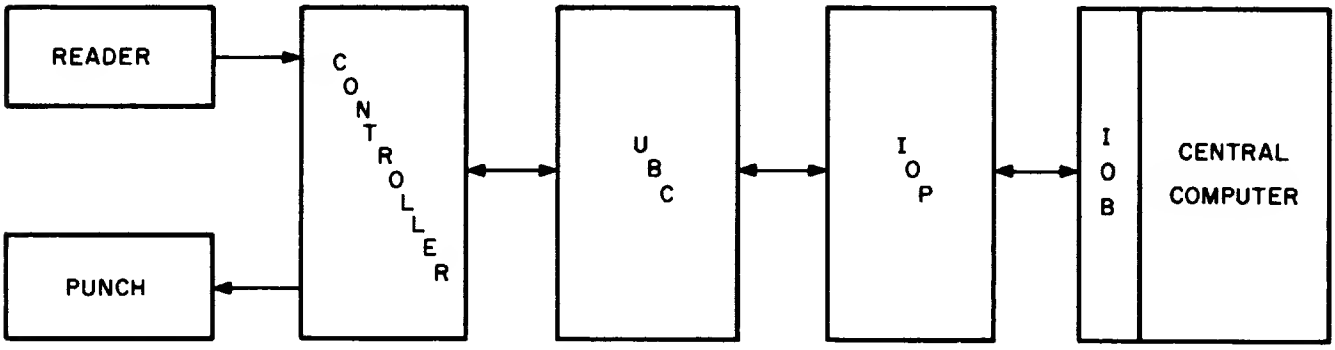


Figure PT-9. Paper Tape System, Model 241, Tie-In With Central Computer

CONTROL DATA

In addition to the AMOUNT OF INFORMATION parameter of the I-O order, the operation of the Model 241 may be controlled with the recognition of a stop character and an end-of-information signal. The stop character may be used in both reading and punching operations, but the end-of-information signal has application only when reading.

The Stop Character

The stop character, octal 72, can be either recognized or ignored during processing operations by the use of the STOP CHAR. switch located on the control panel of the Paper Tape Controller. Separate switches are provided for the reader and for the punch. When recognized, the stop character takes precedence over other control information contained in the Paper Tape Controller. During either a reading or punching operation, if the stop character is recognized before the specified number of words of an order have been transferred, the processing operation stops and the remaining words of the order are not processed.

When the stop character is recognized during a reading operation, the reader stops, and the Paper Tape System is released from its busy status. If 128 words have not been read into the UBC, the Paper Tape Controller generates filler characters to complete the loading cycle of the UBC.

When the stop character is recognized during a punching operation, the punch stops and the Paper Tape System is released from its busy status. If 128 words have not been punched, the UBC completes the unloading cycle although data is not punched.

End of Information Signal

The End of Information signal is represented by at least four blank characters with no sprocket holes and is effective only during the reading operation. When the End of Information signal is sensed, and if 128 words have not been read into the UBC, filler characters generated by the Paper Tape Controller complete the load cycle.

ORDER ACCEPTANCE

The acceptance procedure for I-O orders issued to the Paper Tape System, either on or off line, is performed by the UBC. This procedure is described in detail in the chapter dealing with the UBC.

OPERATING CONTROLS

Registers and controls on the panel of the Paper Tape Controller permit manual control of the processing operation. These registers and controls are the STOP CHAR. switch, the Channel Selection switch, the CONTINUE push button and the Toggle Register.

STOP CHAR. Switch

The STOP CHAR. switch determines whether or not a stop character is to be recognized When the switch is set to OVERRIDE, no check is made for the stop character; when the switch is set to NORMAL, stop characters are recognized.

Channel Selection Switch

The Channel Selection switch is used to select a particular operating mode. Separate switches are provided for the reader and the punch to select any one of the following modes: Five-Channel Binary, Five-Channel Code, Six-Channel, Seven-Channel, and Eight-Channel Image.

CONTINUE Push Button

The CONTINUE push button is used off line to remove error conditions and to allow the reading or punching operations to be continued.

Toggle Register

The Toggle Register is used off line to indicate the number of words to be transmitted to or from the UBC. A stop character overrides the contents of the Toggle Register.

DATA FLOW

Data is transferred between the Paper Tape System and the UBC either a character (Code mode) or two characters (Image mode) at a time. The format of data transmissions is selected with the Channel Selection switch located on the control panel of the Paper Tape Controller. When Eight-Channel Image mode of operation is selected, the format of transmission is two characters at a time; in all other selections, the format is a character at a time.

Reading Operation (See figure PT-10.)

After the format of the transmission has been established and a "run reader" signal is received from the UBC, one frame is read by the reader into the Paper Buffer Register. In this register character parity is checked (when reading seven-level codes) and the presence of a stop character is also determined. When five-, six-, or eight-bit codes are being read, a parity bit is added to the data bits at this point in the operation.

If neither a parity error nor a stop character is detected, a "character available" signal is transmitted by the Paper Tape System to the UBC. On receipt of this signal, the character is moved by the UBC from the Paper Buffer Register into the storage area of the UBC. This action is repeated until one of the following conditions results:

a. end of information is sensed
b. stop character is detected
c. Word Counter equals zero.

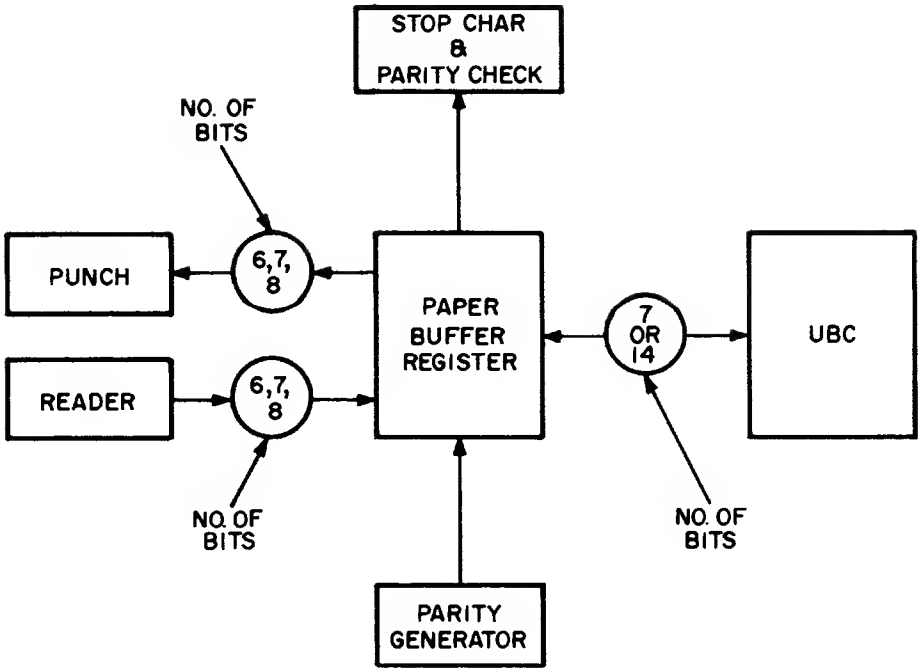


Figure PT-10. Data Flow During Reading Operation, Paper Tape System, Model 241

After 1024 characters (128 words) have been loaded into the storage area, the UBC advances into the unload cycle and tape movement stops.

Punching Operation (See figure PT-10.)

After the format of the transmission has been established, the Paper Tape System waits for the data to be made available by the UBC. When the data is available, the UBC signals the Paper Tape System, and transfers that data into the Paper Buffer Register. In the register, character parity is checked, and the presence of a stop character is determined. The contents of the Paper Buffer Register are then transferred to the punch to be recorded. If seven-level code is being recorded, the six data bits, the parity bit, and the sprocket hole are punched in the tape. When recording five-, six-, or eight-level code only the data bits and the sprocket hole are punched.

Data is transferred from the UBC to the punch in this manner until the Word Counter equals zero or a stop character is sensed.

READING AND PUNCHING EIGHT-CHANNEL TAPE

The format of one word as it appears in the computer memory following a reading of eight-channel tape is illustrated in figure PT-11.

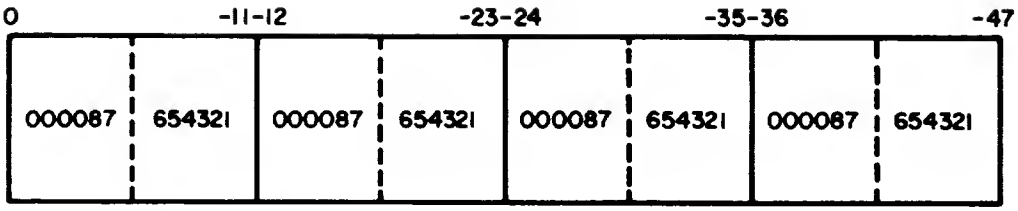


Figure PT-11. Format of One Word in Memory Following a Reading Operation of Eight-Level Tape

In the figure, channels of the paper tape are used to identify the bit positions of each six-bit character of the 48-bit computer word. For convenience, the size of the computer word may now be considered as four 12-bit characters. The four most significant bit positions of each character, therefore, contain zeros.

Before data is punched on eight-channel tape, the programmer must arrange the bits of the computer word (while that word is in memory) into four 12-bit characters containing zeros in the four most significant bit positions of each character. If the format of each word to be processed is not arranged in this manner, data will be lost and a parity error will result.

CHECKING FEATURES

Parity, edit and mechanical faults are checked by the Paper Tape System during the performance of paper tape operations. These faults are indicated on the control panel of the Paper Tape Controller and also on the control panel of the UBC. During on-line processing operations, transmission faults may be checked by interrogating fault registers in the UBC.

Parity Errors

A parity error results when an even number of one-bits in a character are transferred either from the UBC into the Paper Buffer Register or from the Paper Buffer Register into the UBC. If the PARITY OVRD push button on the control panel of the UBC is depressed, the operation continues until the order has been completed. If, however, the push button is not depressed, the operation stops at the end of the block in which the error occured (i.e., 128 words having been transferred).

Edit Errors

An edit error results when more than 128 words are specified by the input-output order (on line); when filler characters are not transmitted by the Paper Tape System when less than 128 words are transferred; or when the setting of the Channel Selection switch does not correspond with the level of tape being punched or read.

When an edit fault is detected, the operation continues until 128 words have been transferred to or from the UBC (load or unload cycle completed).

Mechanical Fault

Mechanical faults result when the Paper Tape System becomes disabled. For example, when the photoelectric reading mechanism is not functioning properly, when the tape is jammed in the punch, if the tape tears, etc. When any mechanical fault develops, the operation stops before completing the transfer of 128 words and the UBC remains electrically connected to the Paper Tape System.

SUMMARY OF OPERATING CHARACTERISTICS, MODEL 241

The operating characteristics of Model 241 are summarized in tables PT-1 and PT-2. Table PT-1 lists the operating characteristics of the tape system when reading, and table PT-2 lists the operating characteristics when punching.

OPERATING CHARACTERISTICS OF PAPER TAPE SYSTEMS

The operating characteristics of the Paper Tape Systems are as follows:

a. Reading speed of 1000 characters per second, with optional speed of 500 characters per second

b. Punching speed of 60 characters per second

c. Starting and stopping on one character

d. Data transmissions of up to 4096 words per instruction with Model 240, and 128 words with Model 241

e. Photoelectric reading.

PHYSICAL CHARACTERISTICS OF PAPER TAPE

The paper tape used with the reader must be opaque, non-oiled, and non-metallic. Reels of either 5-1/2 inch or 7 inch diameter, which hold 350 or 700 feet of tape, respectively, are used.

Tapes with or without metallic strips at the beginning and end of each reel are available. A metallic strip at the end of the tape causes the tape to rewind automatically, and when the tape has been rewound, a metallic strip at the beginning of the reel stops the tape.

The tape used with the punch is mounted on 8-inch reels that hold up to 1000 feet of tape. This permits more than 33 minutes of continuous punching time before a new tape must be mounted. An independently driven take-up reel winds the tape as it is punched. The reel maintains tape tension and automatically shuts the punch off if the tape breaks or if the end of tape is reached and a metallic strip is not present.

TABLE PT-1
READ MODE OF OPERATION

MODE	PARITY CHECK	BLANK TAPE	STOP CHARACTER	BIT INSERTION	FILLER CHARACTERS
Five Channel Binary	No	Interpreted as binary zero	Bypassed. No control characters.	One inserted into sixth position of character	Pure Filler Character. One inserted into sixth position.
Five Channel Code	No	Advanced. No information transmitted	Stops operation. Causes automatic fill of UBC 11010 in figures shift	Zero inserted into sixth position of character	Pure Flller character
Six Channel	No	Interpreted as binary zero	111010 Stops operation. Causes automatic fill of UBC	None	Pure filler character
Seven Channel	Yes. Seventh channel is parity channel. (Odd parity)	Advanced. No information transmitted	111010 Stops operation. Causes automatic fill of UBC	None	Pure filler character
Eight Channel Image	Yes. All eight channels checked for odd parity except for delete (11111111).	Advanced. No information transmitted	111010 in the first six channels. Stops operation. Causes automatic fill of UBC	Four zeros inserted into most significant portion of frame (12 bit).	Pure filler character

TABLE PT-2
PUNCH MODE OF OPERATION

MODE	NUMBER OF BITS PUNCHED	STOP CHARACTER
Five Channel Binary	Five bits of the six-bit character are punched	Ignored. STOP CHAR. BY PASS switch is automatically in operation.
Five Channel Code	Five bits of the six-bit character are punched	11010 Stops operation when in figures shift and STOP CHAR. BY PASS switch is OFF.
Six Channel	Six bits are punched	111010 Stops operation if the STOP CHAR. BY PASS switch is OFF.
Seven Channel	Six bits plus an odd parity bit are punched	11010 Stops operation if the STOP CHAR. BY PASS switch is OFF.
Eight Channel	Eight bits are punched. Four most significant bit positions of frame are ignored but must be zero to avoid parity error.	111010 in six bits. Stops operation in the STOP CHAR. BY PASS switch is OFF.

THE PRINTING SYSTEM

INTRODUCTION

The High-Speed Printing System is operated through the UBC and provides the Philco 2000 computer with a means of producing a printed display of information. Since all printing operations are through the UBC, the information to be printed may be received either on line from the computer memory or off line from another I-O device.

The components of the Printing System include a High-Speed Printer and a Printer Controller; the printer is connected to the controller and the controller is connected to the UBC.

CONTROL CHARACTERS

Three control characters are used by the Printing System; the filler character, the end-of-line character, and the space character. In routine printing operations (Normal mode), 61 of the 64 Philco 2000 characters are printed; the control characters are not printed. A Write All mode of operation may be selected, however, to allow printing of all 64 characters. The Write All mode is selected by depressing the WRITE ALL push button on the control panel of the UBC.

END-OF-LINE CHARACTER

The end-of-line character, octal 77, is represented by the symbol "e". When the end-of-line character is detected, it signifies that the end of information has been reached for one line of printing.

SPACE CHARACTER

The space character, octal 60, is represented by the symbol "Δ". When this character is encountered, it is not printed, and the space that the character would have occupied is left blank.

FILLER CHARACTER

The filler character, octal 32, is represented by the symbol "n". When the filler character is encountered, it is not printed, but is replaced by the character that follows it.

DATA FORMAT

Printing is performed a line at a time, and in Normal mode any number of characters up to 120 may be printed on one line. The standard format of each line of printing is as follows:

VS xxx...xxx e

120 characters
Normal Mode

Where: V represents the first character of each line and is used to specify the vertical format of that line.

S represents the second character of each line and is used to specify the Data Select, Conditional Stop, or Absolute Stop characters that are used by the UBC. These characters are ignored by the Printing System.

e represents the last character of the line, and is used to specify when the end of information has been reached.

VERTICAL FORMAT

Paper in the printer is advanced according to the vertical format character, which is called the line feed character. The line feed character is always the first character of a line, and should always be the first character following an end-of-line character. When the end-of-line character is sensed, it indicates that the end of data for that line of printing has been reached. The next character that is translated by the controller is assumed to be the vertical format character for the next line of printing.

There are seven acceptable line feed characters which are represented by the Philco 2000 characters 1 through 7. Each line feed character corresponds to a channel of a seven-channel paper tape loop, which is read by a small paper tape reader located in the printer. (See figure PR-1.)

The loop is moved synchronously with the paper in the printer. When a line feed character is detected by the Printer Controller, the loop and the paper are advanced until a hole

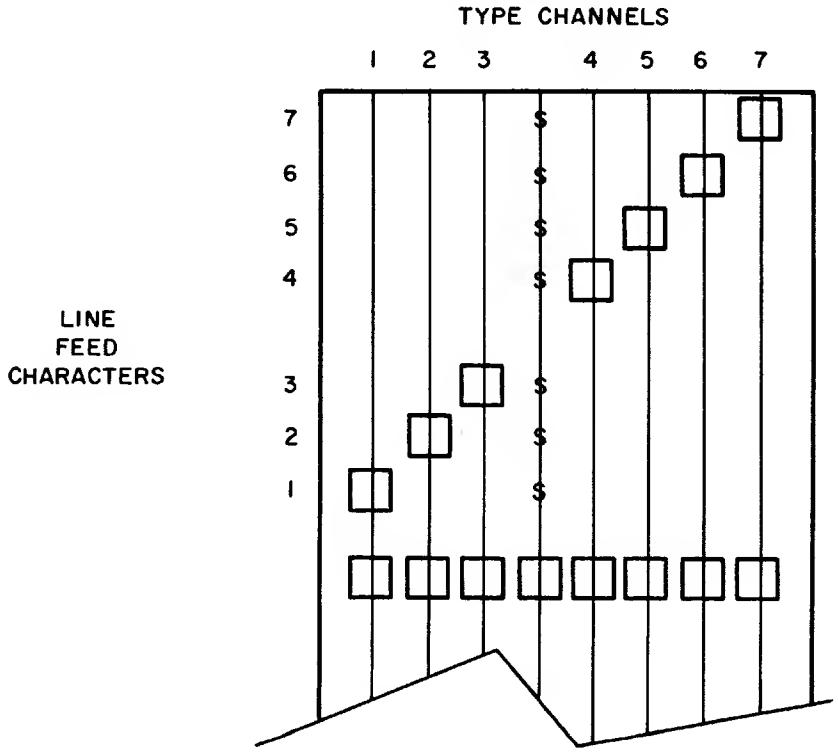


Figure PR-1. Vertical Format Tape Loop

is detected in the channel of the loop which corresponds to that character. Then the paper and the loop stop, and printing takes place on that line. The distance between the printed lines, therefore, depends upon the pattern of punches in the channels of the loop and specified line feed characters.

The paper is not advanced when there is a zero in the first character position, or line feed character position, of a line. Such a line will then be printed superimposed on the previous line. In this way, combinations of characters may be printed; the line may be made darker for emphasis; or two or more lines which have information in different columns may be combined, for example, totals and subtotals.

In order to protect the paper and the ribbon of the printer, both must be advanced at least once for every seven lines printed. If seven lines are superimposed on one another, the printing operation will stop after the seventh line is printed.

If a legitimate vertical format character is detected and there is no hole in the corresponding channel of the vertical format tape loop, the paper and the loop will continue to feed until they are stopped by the operator. Therefore, every loop should have one frame which contains a hole in each channel, even though a line feed character corresponding to those channels may not be used during the printing operation.

When any character other than a legitimate vertical format character is in the line feed position (first character of a line), the Printer Controller will assume the vertical format to be 1, or a line at a time.

If the vertical format tape loop should tear, or not be placed in the reader, the printer will perform single line advances whenever any legitimate line feed character is detected.

If only one line of data is to be fed to the printer, a vertical format character and a corresponding punch in the tape loop must still be provided.

HORIZONTAL FORMAT

The format of the printed line is controlled during normal printing operations by the control characters, and in all operating modes by a plugboard. Following the first two characters of each line, all characters are checked to determine whether or not they are control characters. If a control character is detected, and if that character is a filler or an end-of-line character, it is not printed and is not counted as one of the possible 120 characters which may be contained on one line of printing. If the character is a space character, it is not printed; however, it is counted and its position on the line is left blank. Characters other than control characters are sent as they are examined to the next available character position on the line. When either the end-of-line character is detected or 120 characters have been counted, no further characters are examined for that line, and that line is printed.

As each line of data is sent to the printer, it passes through a plugboard which allows the format of the line to be altered. The printer plugboard is usually wired one-to-one. That is, the first character sent to the printer is entered in character position (column) one of the line, the second character is printed in position two, and the third is printed in position three, etc., until up to 120 characters have been printed or the end-of-line character

is detected. By rearranging the jumper wiring of the plugboard, any character may be printed in any desired character position on the line, and any character may be repeated up to four times on a line. The plugboard is illustrated and described in the Operating Controls Manual TM6.

HIGH-SPEED PRINTER LAYOUT SHEET (See figure PR-2)

A printer form called the "High-Speed Printer Layout", GI 419, is provided as an aid to the programmer in arranging the material to be printed and in preparing a vertical format tape loop. On the sheet, the number of characters per line is indicated at the top and the number of lines per page is indicated at the side.

The vertical format tape loop is shown at the extreme right side of the sheet as a rectangular block. The small block area above the tape loop shows the channels of the tape loop which will be punched by pressing the designated keys of either the Console Typewriter or the Paper Tape Punch.

When using the sheet, each line of data should be arranged in a horizontal line, with each character of that data occupying a single block of the horizontal line. The number indicating the vertical tape loop channel to be punched should be placed in the rectangle representing the tape loop, opposite the line of data.

For example, if the programmer wished to write the phrase, PHILCO FAMOUS FOR QUALITY THE WORLD OVER, on the right side of the page, skip five lines and write the phrase a second time, skip one line and write the phrase a third time, it would appear on the layout sheet as shown in figure PR-3.

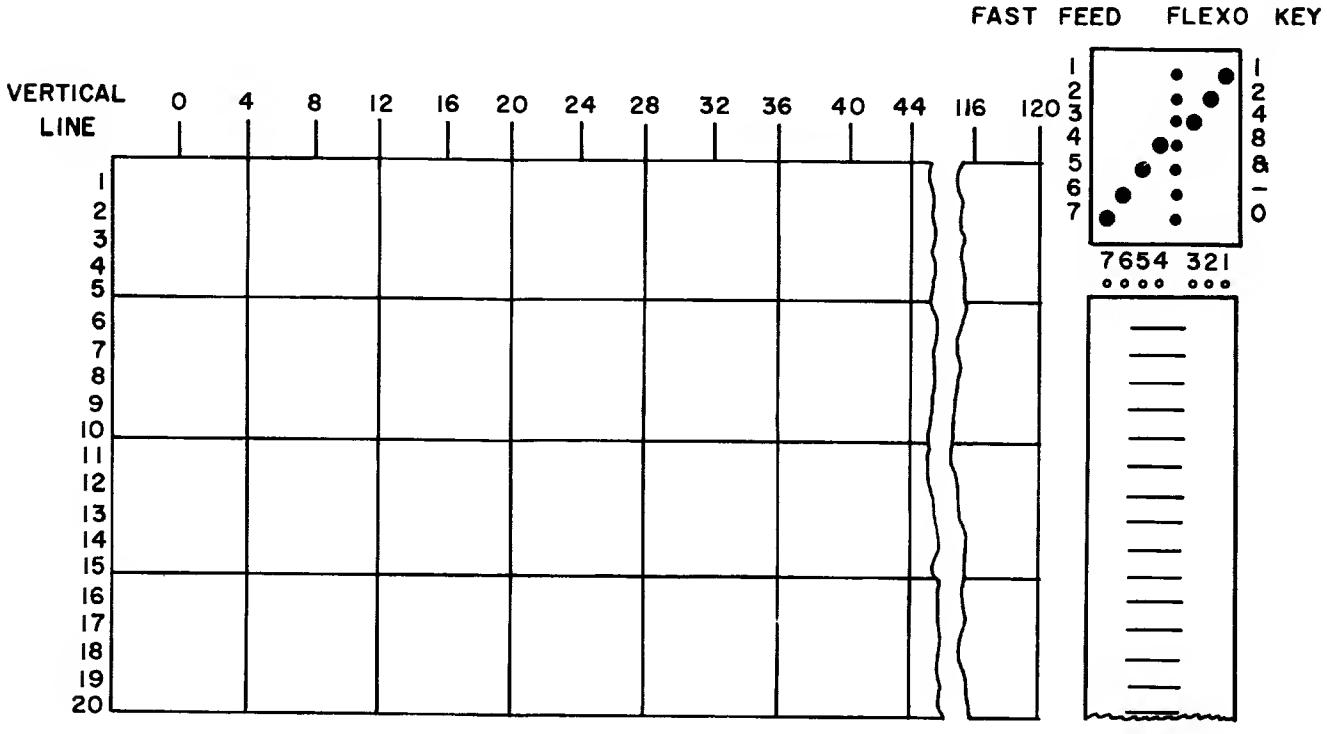


Figure PR-2. High-Speed Printer Layout

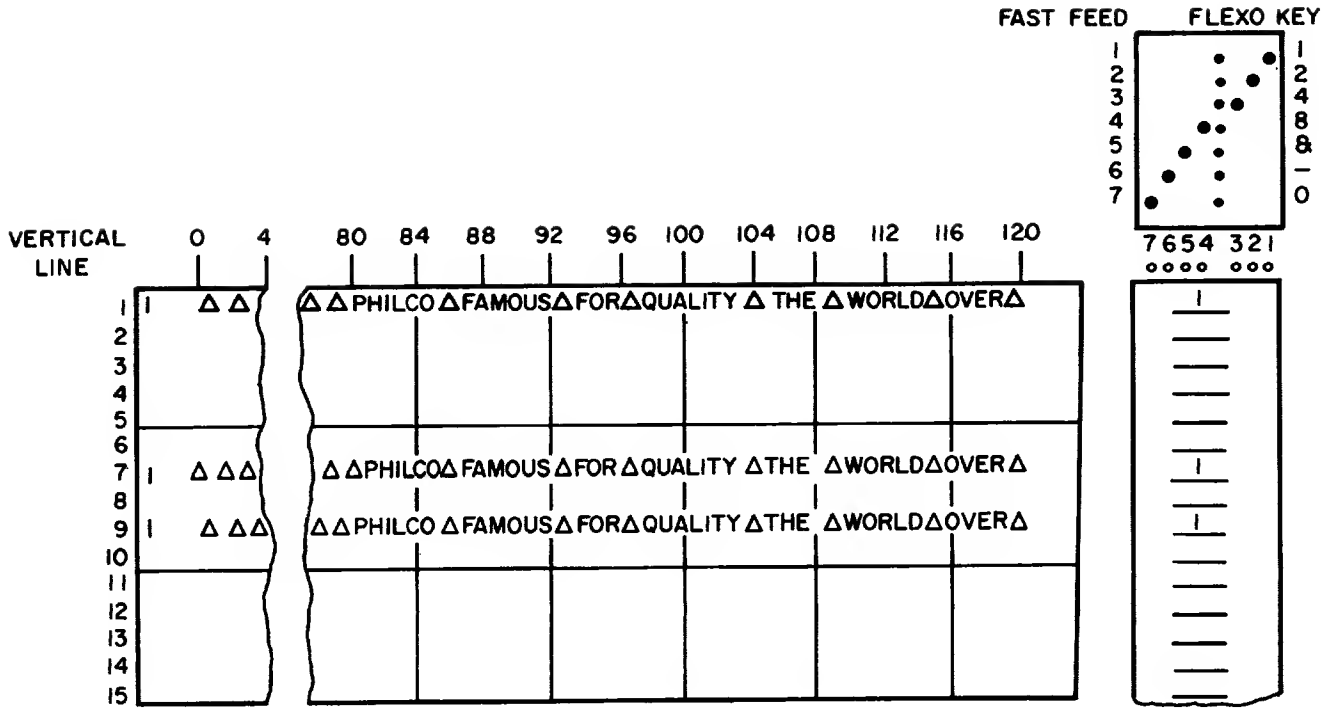


Figure PR-3. Use of Printer Layout Sheet

The vertical format character chosen in this example is "one". At the left of the zero line on the layout sheet, four spaces are available to allow the vertical format character and the Data Select code to be entered. Therefore, the vertical format character "one" can be placed into one of these four spaces indicating that the line will be printed when a hole in channel one of the vertical format tape loop is sensed. The line is then filled with space characters, starting with the first block to the right of the zero line and continuing until the block containing the 80th character is reached. The phrase is written out, including the space characters between each word, until the 121st block is reached. In this block, the end-of-line character must be entered. A one is written in the rectangle (representing the tape loop) at the right side of the sheet opposite line one to indicate that channel one of the tape loop must be punched in order to correspond with the vertical format character being used for that line. Five lines are skipped and the writing of the vertical format character and the phrase is repeated in line seven. A one is written in the rectangle opposite line seven; this indicates to the programmer that five lines are to be skipped on the tape loop before another punch is placed in channel one of the tape loop. Two lines are skipped. The vertical format character "one" is entered and the phrase is repeated in line nine. A one is placed in the rectangle opposite line nine. This indicates that one line is skipped before another punch is placed in channel one of the tape loop.

In this way the phrase is printed, five lines are skipped and the phrase is printed again, two lines are skipped and the phrase is printed a third time. A vertical tape loop can now be prepared to correspond with the desired format of data contained on the layout sheet. It should be noted, however, that this example does not illustrate all the coding necessary to produce an error-free printout. It is intended merely as an aid in developing an approach to arranging data on the layout sheet because the print-out will vary depending upon the particular installation.

ORDER ACCEPTANCE

The acceptance of all I-O orders issued to the Printing System, either on line or off line, is controlled by the UBC. The acceptance procedure followed by the UBC is explained in detail in the chapter on the UBC. In brief, however, both the UBC and the Printing System must be non-busy and mechanically available before an order will be accepted.

DATA FLOW (See figure PR-4)

Data is transmitted seven bits at a time from the UBC into a decoding network in the Printer Controller where character parity is checked, the parity bit deleted, and the six data bits examined for the presence of a control or format character. If the six data bits are not control or format characters, they are transferred to a Line Buffer Register, which stores characters until one line of printing has been formed. This is indicated either when an end-of-line character is sensed, or after the 120th character has been counted and read into the Line Buffer Register.

If the character examined is a filler character, it is deleted; if an end-of-line character is sensed, the line buffer is unloaded through a plugboard to the printer and the printing phase begins. The character following the end-of-line character is examined for the presence of a vertical format code and then sent to the paper tape reader in the printer. The second character following the end-of-line character is ignored by the Printer Controller. This character is the Data Select code and is meaningful only to the UBC during off-line applications.

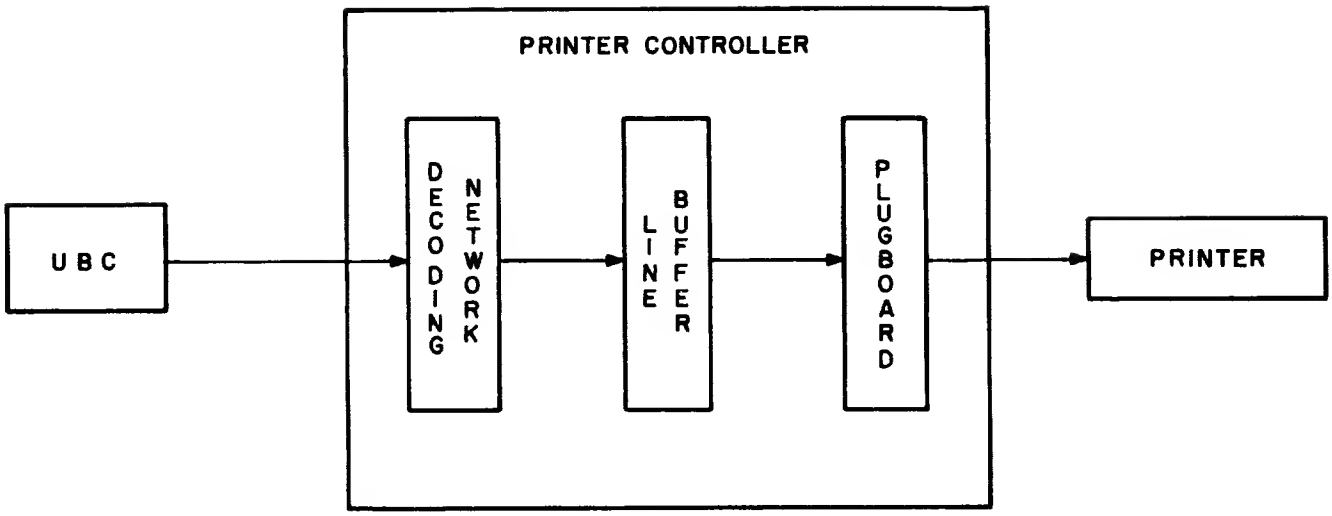


Figure PR-4. Data Flow during a Printing Operation

PRINTING CYCLE

There are 120 printing positions on a continuously revolving print roll, and each printing position contains 64 Philco 2000 characters embossed on the circumference of the roll. (See figure PR-5.) During the printing phase, as the roll revolves, the characters in the line buffer are matched with the characters on the print roll. If any characters match, the impulse leaves the line buffer from those positions and passes through the plugboard to the printer. The impulses fire thyratrons, which provide power for the print hammers to strike the paper. There are 120 thyratrons, one for each print position. As the thyratron is fired, the hammer strikes the paper and the paper is forced against the ribbon, which, in turn, is forced against the print roll to cause that character to be printed.

After a line has been printed, the paper is advanced according to the programmed vertical format. While the paper is advancing, the line buffer is loaded with a new line of data.

OPERATING MODES

The Printing System may be operated in any one of three different modes, a Normal mode, a Write All mode, and a Test mode.

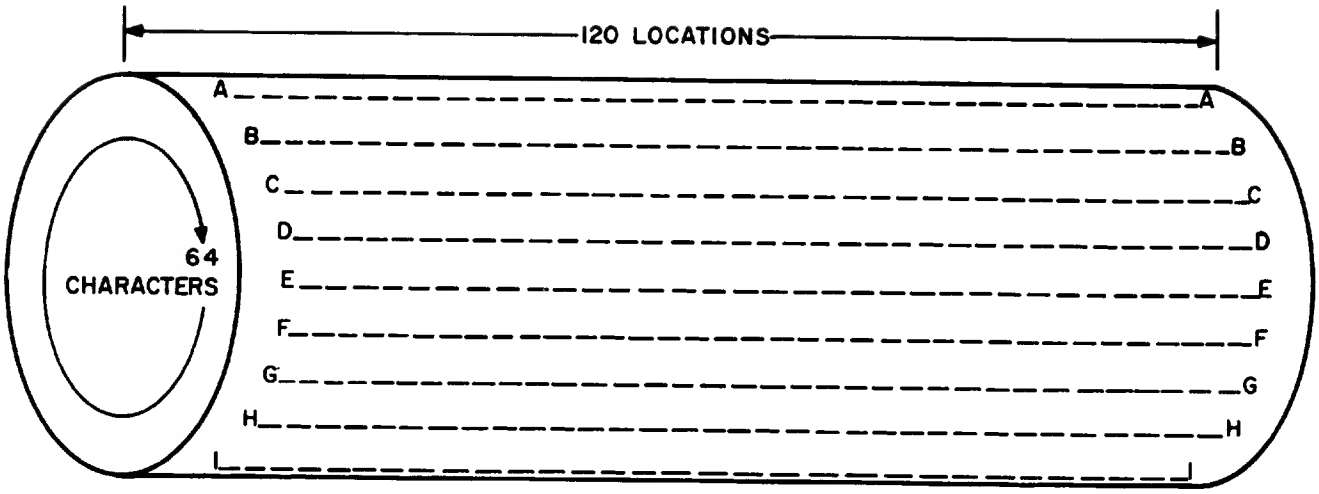


Figure PR-5. Print Roll of High-Speed Printer

NORMAL MODE

The Normal mode is used for routine printing functions. That is, when the Printing System is being used either on or off line and when control characters and line feed characters are being used to control the format in which data will be displayed.

WRITE ALL MODE

The Write All mode is used when a memory dump is to be performed. This mode enables all 64 of the Philco 2000 characters to be printed.

In Write All mode, the Printer Controller does not check for control characters. The line buffer is filled sequentially with 64 or 80 characters per line from the UBC. The paper advances a line at a time.

The selection of the Write All mode is made by depressing the WRITE ALL push button on the control panel of the UBC.

The selection of 64 of 80 characters is made by a switch on the Printer Controller. The 80-character position permits the contents of punched-cards to be printed without computer or plugboard editing.

When the switch is in the 80-character position, each block is printed on 13 lines. The first twelve lines contain ten words each. The last line contains the last eight words of the block, taken from the first 64 positions of the line buffer. The first character of the next block starts the next line.

TEST MODE

The TEST MODE switch on the Printer Controller panel permits off-line printing of any selected character in all 120 columns. The character is selected by six toggle switches, and no input is needed from the UBC. The paper is advanced a line at a time in this mode.

CHECKING FEATURES

In the Normal mode of operation, the Printer Controller checks for parity, edit, and mechanical faults which may occur during a printing operation. These faults are indicated on the control panel of the UBC and also on the Printer Controller panel. Off line, an error condition will cause the printer to stop before the printing operation has been completed. On line, the printing operation is controlled by the UBC and only mechanical faults occuring in the Printing System will cause the printer to stop. The Fault Register of the UBC may be interrogated to determine the status of transmissions to the Printing System when the printer is being operated on line.

PARITY ERROR CONDITIONS

If a character parity error is detected during the printing operation, the printer stops following the loading of the line buffer, and the PARITY ERROR indicator on the Printer Controller lights. The line containing the character in error will remain in the line buffer and will not be printed.

EDIT FAULT CONDITIONS

Off line, the following conditions will cause the printer to stop and the EDIT ERROR indicator on the Printer Controller panel to light:

a. the character following the 120th character of a line is not an end-of-line character

b. the last character in a block is not an end-of-line character.

If more than 120 characters are sent to the line buffer before end-of-line character is detected, the printer will stop and the line will not be printed. On line, if either the 121st or 122nd character is not an end-of-line, the EDIT ERROR indicator lights and the 122nd character is assumed to be the end-of-line character. When this condition occurs, the information following the 120th character (the next two characters) is lost.

The last character in the block being printed must be an end-of-line character. If the number of printing and control characters in a block does not equal 1024, filler characters should be inserted after the last character to be printed, up to, but not including, the last character. The last character should then be made the end-of-line character. If the last character in a block is not an end-of-line character, the printer will stop and the last line will remain in the line buffer. (On line, the printing operation will continue and the printer will be released from the UBC.)

MECHANICAL FAULTS

The following conditions require operator intervention and cause the printer to stop and an appropriate indicator on the Printer Controller panel to light, regardless of the operating mode and on/off line status:

a. the paper supply is torn or exhausted

b. the circuit for a print hammer has become inoperative

c. the print ribbon is out of line with the print hammers

d. overprinting occurs more than seven times on one line.

OPERATING CONTROLS

Two toggle switches on the Printer Controller, called the EDIT ERROR OVERRIDE and the PARITY CHECK OVERRIDE, are provided to permit manual control of off-line printing operations. When these switches are in the OVERRIDE position, they permit the printing operations to be continued if a parity or edit error is detected.

CHARACTERISTICS OF THE HIGH-SPEED PRINTING SYSTEM

The operating characteristics of the High-Speed Printing System are as follows:

a. Printing rate of 900 lines per minute

b. Skipping rate of 9000 lines per minute

c. Sixty-four printable characters

d. Data Format — 120 characters per line, ten characters per inch horizontally, six or eight lines per inch vertically

e. Number of copies — original and five carbon copies.

MAGNETIC DRUM SYSTEM

INTRODUCTION

Auxiliary storage in the 2000 series is provided by the Magnetic Drum System, a large capacity, random access, input-output device. A Magnetic Drum System is capable of supplementing the 2000 memory with 32,768 storage locations.

A drum system consists of a drum controller and a magnetic drum; the drum is connected to the controller and the controller is connected to memory through the IOB.

DATA FORMAT (See figure DR-1)

The 48-bits of each computer word are stored on the surface of the drum as small magnetized areas. The drum surface contains eight bands, and each band is divided into 4096 distinct locations. (It is not necessary for the drum to contain the maximum of eight bands.) In turn, each location has 48 individual magnetizable areas where the bits of a computer word are stored. One band on the drum, therefore, may contain as many as 4096 computer words.

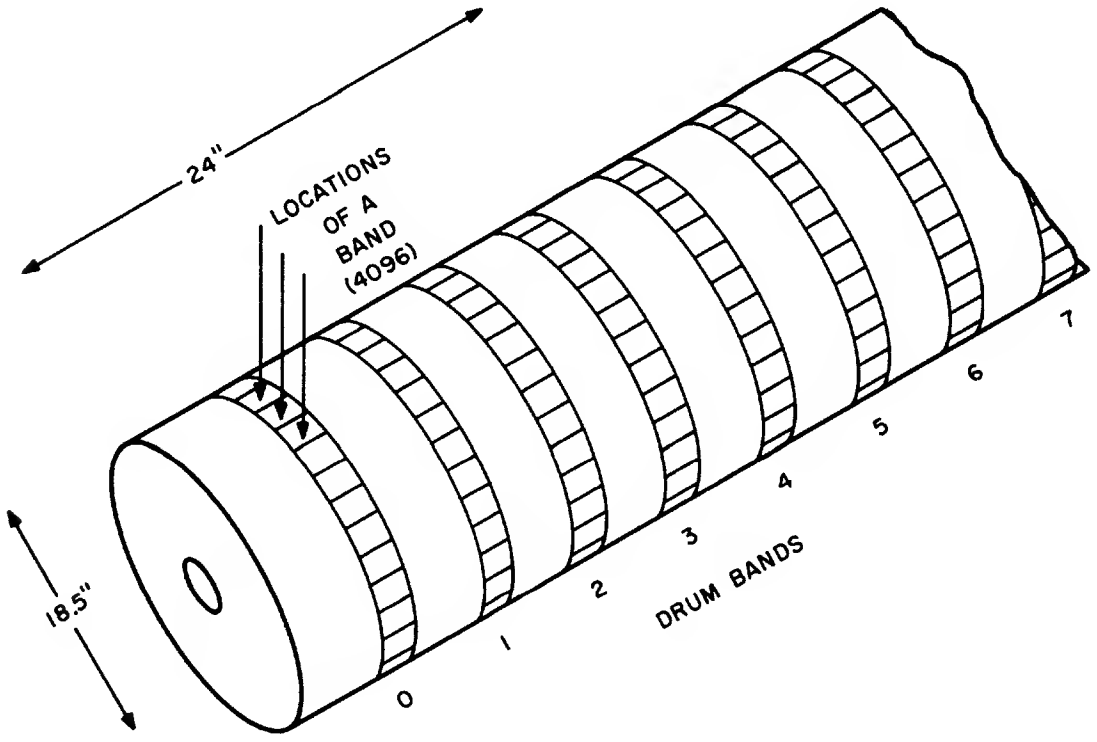


Figure DR-1. Simplified Drawing of Drum Showing Drum Bands and Data Locations of These Bands

Reading and writing on the drum is performed with read/write heads. In total, one drum may contain up to 384 of these heads.

The magnetic drum is a rotating cylinder 18. 5 inches in diameter, and 24 inches long. It is rotated in a hollow cylindrical housing on which the read/write heads for each band are mounted. As the drum bands pass under the heads, data is transferred to or from the data locations of the band.

The drum is rotated in the housing at a controlled speed of 1750 rpm. This high speed moves sequential data locations of the band under the read/write heads once every eight microseconds. The average memory access time of the Central Computer, Models 210 and 211, however, is 10 microseconds. This means that the computer memory cannot be accessed in time to read or record data in sequential locations of the band; therefore, data is recorded in alternate locations and two complete drum revolutions are required to process data in all 4096 band locations. This method of reading and recording data is referred to as interlacing, and is illustrated in figure DR-2. The process of assigning band locations to sequential words is a function of the drum controller. The programmer need not be concerned with this process, because I-O orders need to contain only the sequential address of the word and not the band location.

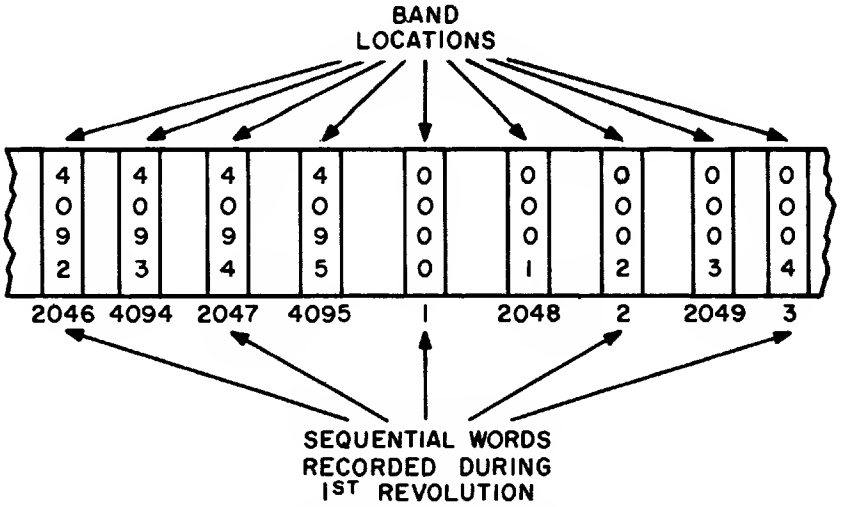


Figure DR-2. Section of Drum Band Showing Band Locations and Sequential Words Recorded in These Locations

ORDER ACCEPTANCE

In the Input-Output Section, the Magnetic Drum System is unique in its acceptance requirements and its operating characteristics. Before a magnetic drum order can be accepted, all other input-output systems must be non-busy, and the drum system must be mechanically available. Furthermore, after a drum order has been accepted, the computer memory cannot be accessed by the Central Computer until the drum order has been completed. This operating characteristic of the drum system prevents the Central Computer from continuing with the main program, during drum orders, and is a result of the intense speed of transmission between the drum and the computer memory. The period of time during which the computer memory remains non-accessible is referred to as "drum seizure." (If the drum order were to specify the transfer of 4096 words, the maximum

allowable per order, the time required to complete the operation would only be 66 milliseconds, not including drum band and band locations accessing time.)

When an I-O order addressing the drum system is issued, it is decoded in the Central Computer, and, if another I-O order is not being performed by an I-O device, the drum order is allowed to continue to the drum controller. In the controller, the mechanical availability of the drum system is determined. (See figure DR-3.)

If another I-O device were busy or if the drum system were mechanically unavailable, the order would not be accepted, and the next instruction in the main computer program would be executed. If, however, the order is accepted, it must be completed before the computer can continue with the main program; that is, in order for the computer to skip the next instruction and proceed.

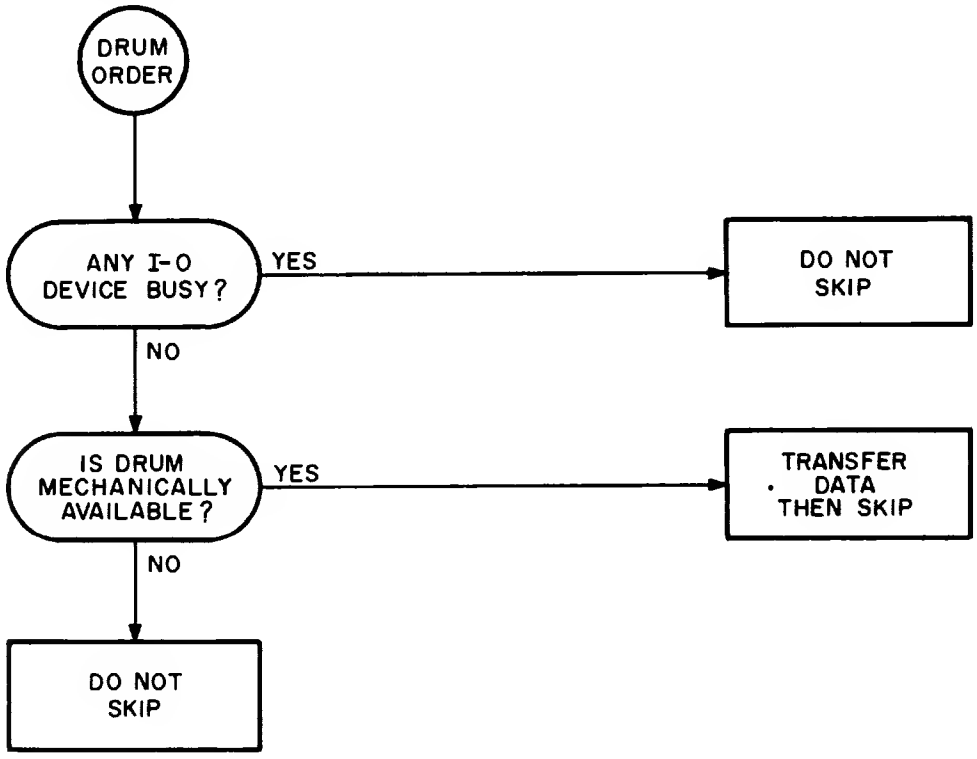


Figure DR-3. Flowchart of Drum Order Acceptance Procedure

DRUM OPERATION

Any number of words from 1 to 4096 may be specified when reading or writing on the drum, and the operation may start at any data location of a drum band.

After a drum order is accepted, the contents of the D Register are transferred into appropriate registers in the drum controller, and these registers control the transfer operation. Before a transmission begins, the activity in the drum controller includes selecting the desired drum and the band of that drum, establishing the circuitry necessary for the read/write heads of the band, and initiating the data transfer when the location on that band containing the first word of the transfer comes under the read/write heads.

The average access time to complete these functions is approximately 17 milliseconds (maximum time is 34 milliseconds).

A word counter located in the Central Computer receives the contents of the field in the D Register which specifies the number of words to be transferred. The word counter is decremented by one as each word is transferred, and when the word counter equals zero, the transmission stops.

READING OPERATION (See figure DR-4.)

Data is read from the drum one word, 48 bits, at a time. As alternate data locations of the band pass under the read/write heads, the magnetized areas are translated into electrical pulses. The pulses are then fed to 48 read amplifiers contained in the drum controller. These amplifiers are switched between the read/write heads of all the bands of every drum and, at any one time, can only be used with the drum band being accessed.

After the pulses are amplified, they are sent to the IOB, and from the IOB they are placed into the computer memory.

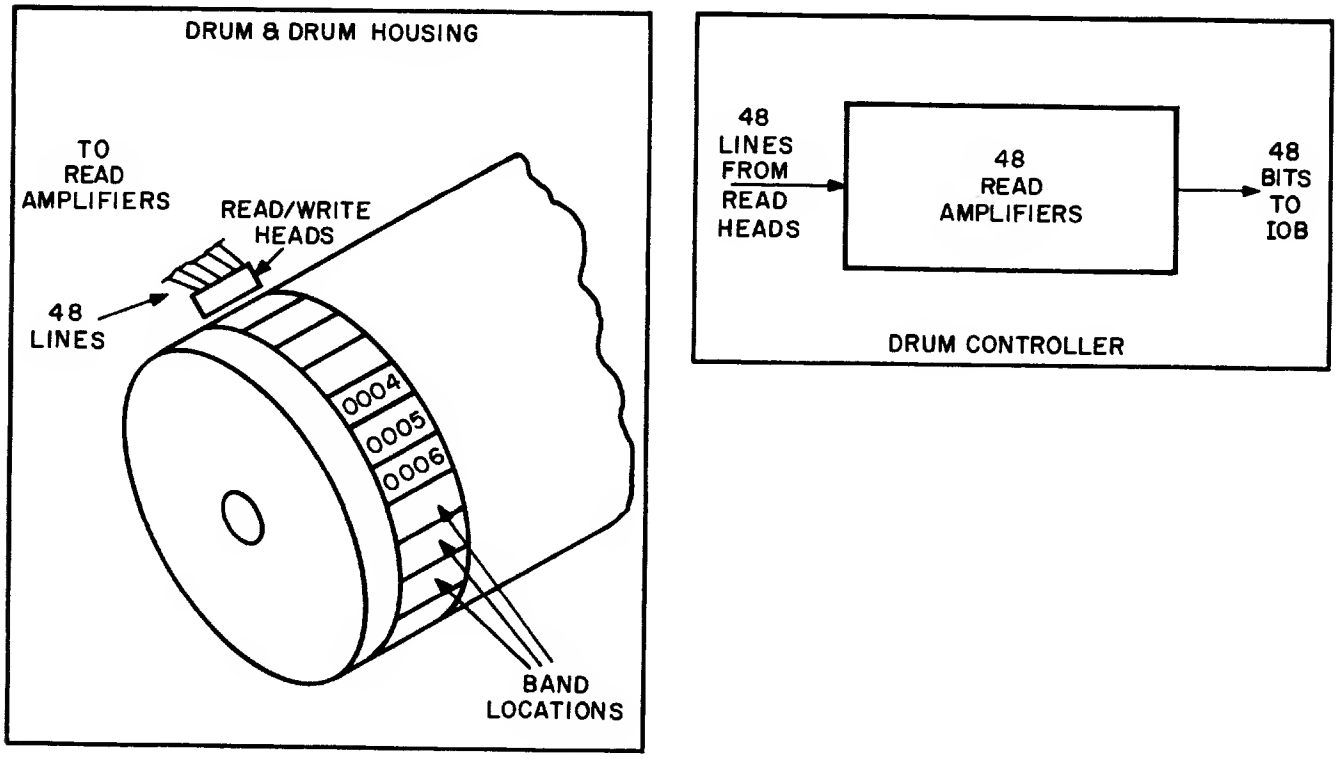


Figure DR-4. Data Flow During Reading Operation

WRITING OPERATION (See figure DR-5.)

Data is recorded on the drum one word, 48 bits, at a time. The word is transferred from the computer memory into the IOB, and from the IOB into 48 write amplifiers contained in the drum controller. These amplifiers are switched between the read/write heads of all the bands and at any one time can only be used with the drum band being accessed.

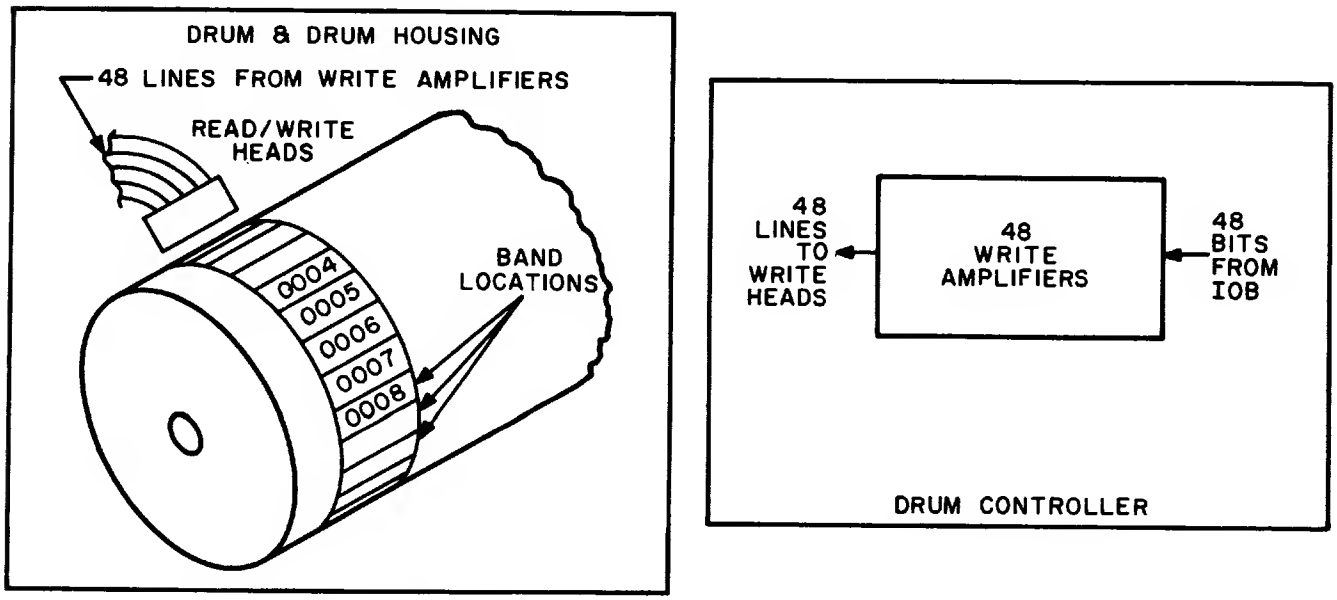


Figure DR-5. Data Flow During Writing Operation

After the pulses are amplified, they are fed to the write heads of the band. The current through the write heads creates a magnetic field which magnetizes each area of the band location passing under the write head. The direction of the flux field of the area magnetized distinguishes between a 1 and 0 bit; that is, the flux field representing a 1 bit would be in the direction opposite to the flux field representing an 0 bit. The direction of current through the write head determines the direction of the flux field. (See figure DR-6.)

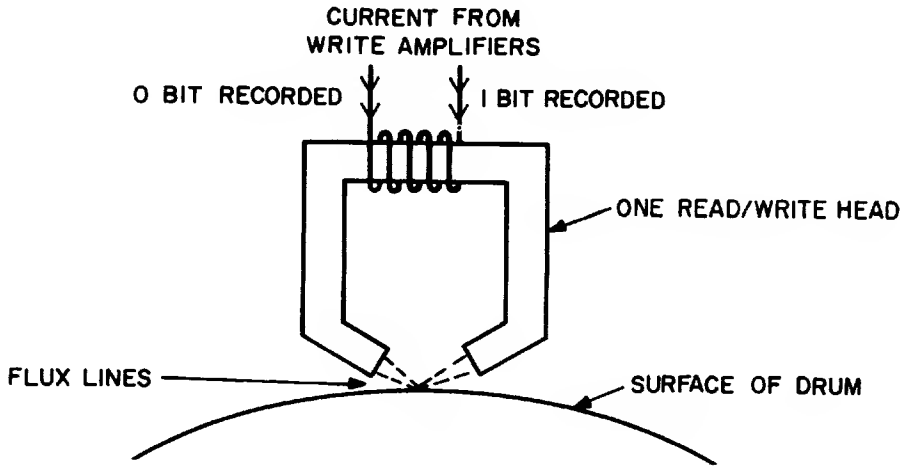


Figure DR-6. Writing Method for 1 and 0 Bits

BAND SWITCHING

If the number of words to be transferred exceeds data location 4095 of the specified band, the drum system switches automatically to location 0000 of the next higher drum band to complete the order.

The bands are numbered zero through seven. During the time interval required to complete the band switching, data is not transferred. The average time required to actuate the necessary band switching relay is eight milliseconds.

CHECKING FEATURES

The magnetic drum contains automatic checking features which constantly monitor the drum activity. These checking features test for correct drum rotation speed, and for correct reading of information from the drum. The faults are displayed by a two-bit fault register in the drum controller. One of the two bits indicates that the word at band location 0000 does not appear at the reading heads at the proper time; this is referred to as a location fault. The other bit indicates that all 48 bits of the computer word have not been sensed by the read heads; this is referred to as a reading fault.

If a location fault occurs during writing operations, the drum order is terminated at the point in the operation at which the error occurs. If a reading fault occurs, the order is not terminated. Instead, the operation continues until the order is completed.

Following either the termination or completion of a drum order, the drum system transmits a "continue" signal to the Central Computer. When this signal is received by the computer, the instruction following the TIO instruction is skipped, and the computer continues with the main program. In either case, the drum order will appear to be completed. A skip instruction should be coded following all drum orders to check the reliability of transmission to and from the drum.

WRITE DISABLE

A "write disable" feature guarantees permanent storage of data on a drum. A write-disabled drum may have data read from it but may not have data written onto it. If an attempt is made to write on a write-disable drum, the order will be accepted, and a location fault will be indicated.

Push buttons on the drum controller are used to write disable a drum. The possible combinations for any drum controller are as follows:

a. all bands may be write disabled

b. any one or more bands of a drum may be write disabled

OPERATING CHARACTERISTICS

The operating characteristics of the Magnetic Drum System are listed as follows:

a. Capacity of 32,768 words

b. Transfer rate of 500,000 characters per second

c. Processes over 4,000 words per order

d. Access time — 25 milliseconds for the first word and 17 microseconds for each succeeding word

e. Type of Transmission — 48 bits in parallel.

THE REAL-TIME SYSTEM

INTRODUCTION

Real-time inputs are supplied to the Philco 2000 by the Real-Time System, which consists of an Auto-Control Unit with a built-in Real-Time Scanner, and an optional unit, an interval timer. Other devices, such as radar and teletype, may also be coupled to the Real-Time System.

The Real-Time Scanner is provided to multiplex one, four, or eight real-time units, including the Auto-Control Unit, and to provide a means of checking these units.

The Interval Timer Unit (Timer) provides a time reference for the Philco 2000, thereby facilitating the interlacing of programs and the timing of critical operating intervals. The Timer is a millisecond clock which allows intervals up to nine hours in duration to be timed and interrogated.

The Auto-Control Unit (ACU) provides a means of interrupting a program whenever previously determined conditions appear in either the Philco 2000 Central Computer or in the Philco 2000 Input-Output System. This interrupt feature is completely under program control and permits the programmer to determine the system conditions that shall be checked, when these conditions shall be checked, and what action is to be taken when these conditions are present.

SYSTEM TIE-IN (See figure RT-1)

Both the Interval Timer and the Auto-Control Unit are connected to the IOB through the Real-Time Scanner, which is connected to the IOB through the Real-Time Channel. The ACU may receive signals from any input-output device or from the Central Computer; when these signals are received, the information is transferred through the Real-Time Scanner to the Central Computer.

The Timer transfers its information to and from the Central Computer through the Real-Time Scanner. When an Auto-Control Unit is connected to the Timer, the program can be interrupted after a designated period of time set in the Timer. When an Auto-Control Unit is not connected, the program may not be interrupted after a designated time interval, but it is still possible to obtain a time reference readout from the Timer.

FUNCTIONAL DESCRIPTION OF THE REAL-TIME SCANNER

The primary function of the Real-Time Scanner is to transmit the parameters of the real-time input-output order to the designated real-time device and to transfer information between the Central Computer and that device. First, the real-time input-output order is placed in the D Register; the TIO is then issued. If the TIO is accepted, the parameters

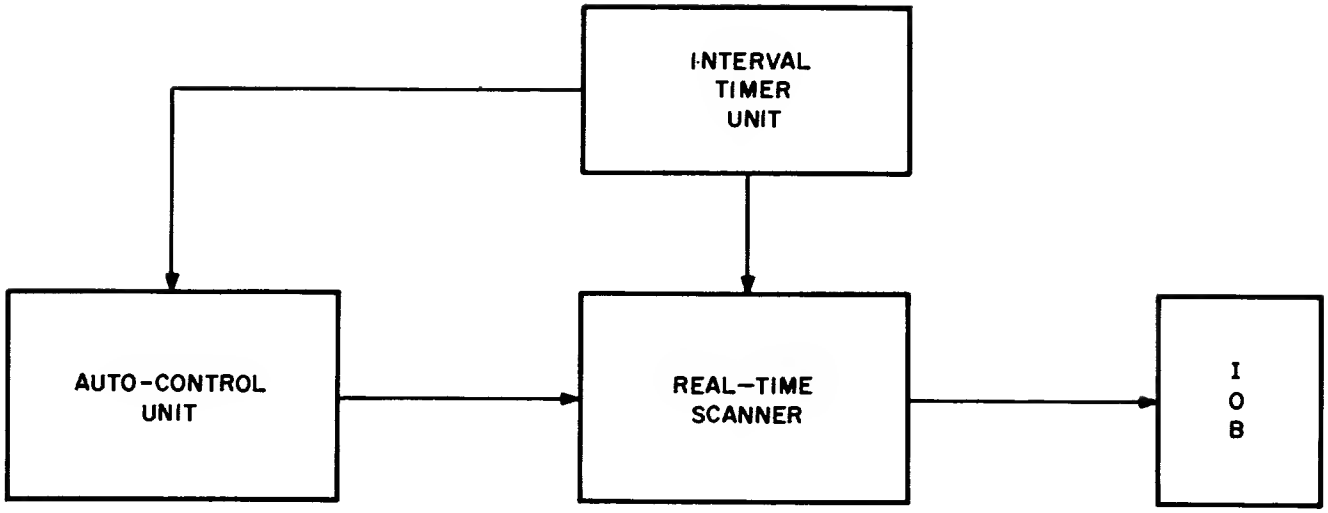


Figure RT-1. Real-Time System, Simplified Block Diagram

of the order are sent to the Real-Time Scanner. The Real-Time Scanner then transfers the parameters to the unit specified by the UNIT field of the TIO instruction. The parameters are as follows:

a. command, sets the unit in either input or output mode of operation

b. amount of data to be transferred

c. address of the first memory location to be accessed (obtained from the ADDRESS field of the TIO instruction).

The Real-Time Scanner then interrogates in turn, each unit that is connected to it. When the unit is ready to receive or transmit information, one word is transferred between memory and the designated real-time unit. This action continues until all real-time orders are completed.

FUNCTIONAL DESCRIPTION OF THE AUTO-CONTROL UNIT

MAJOR COMPONENTS OF THE AUTO-CONTROL UNIT

The Auto-Control Unit (ACU) contains two data registers. (See figure RT-2.) One of these registers, the Auto-Control Register (AC REG.), is a 48-bit register which indicates a designated status change within the computing system. Each condition to be checked is represented by one bit in the register. The other register, a 48-bit mask register, determines the bits in the Auto-Control Register that are transferred to memory, and this determines the specific conditions that are to be checked by the ACU. The bit configuration in the mask register is transferred from memory to the ACU when the auto-control order is accepted.

In addition to the two data registers, the ACU contains one control register, the AC MA Register, which contains the following information:

a. address of the memory location to which the contents of the Auto-Control Register are transferred (M + 1)

b. address of the memory location to which the contents of the JA Register are transferred (M + 2)

c. address of the memory location which contains the first instruction of the executive routine (M + 3).

The AC MA Register normally contains M + 1. The register is incremented each time it is used to form the addresses M + 2 and M + 3.

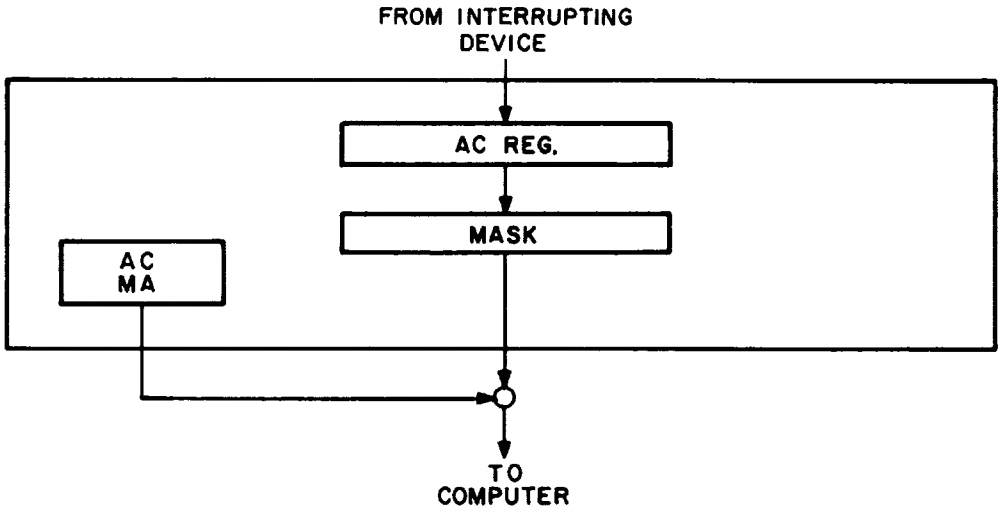


Figure RT-2. Registers of Auto-Control Unit

PROGRAMMING THE AUTO-CONTROL UNIT

The I-O order which addresses the Auto-Control Unit is brought into the D Register, and a TIO instruction is then issued. (See figure RT-3.) If the TIO is not accepted, the program continues with the next instruction in the program. If the TIO is accepted, one instruction is skipped and the main program continues. After the TIO is accepted, the word in the memory location specified by the address portion of the TIO instruction (M) is transferred to the auto-control mask register. The address portion of the TIO is then increased by one (M + 1), and this new address is transferred to the AC MA Register. The inhibit, which kept the program from being interrupted, is then removed, and the ACU is set up to interrupt the program when a specified condition occurs.

OPERATION OF THE AUTO-CONTROL UNIT

Whenever a specified condition is present in the computing system, a specified bit is set to one in the Auto-Control Register. (See figure RT-4.) If the corresponding bit position in the mask register contains a one, the auto-control word is transferred to memory location

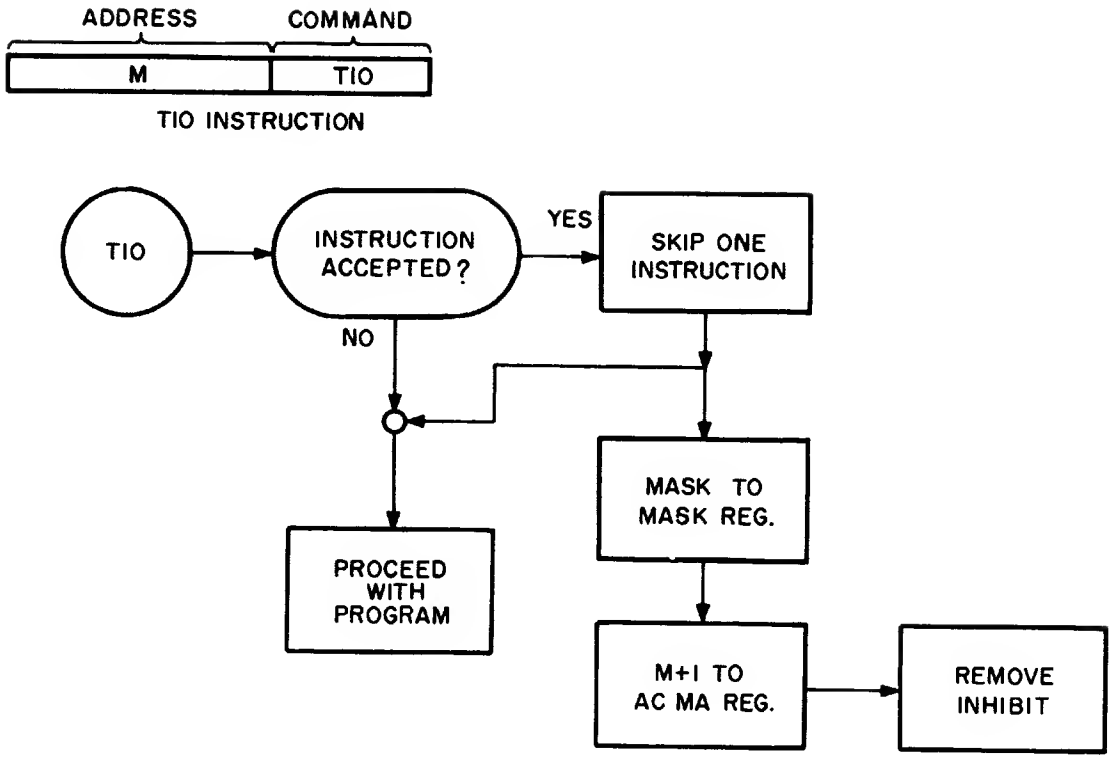


Figure RT-3. Setup of Auto-Control Unit

M + 1. After the auto-control word has been transferred to memory, the masked bits in the Auto-Control Register are cleared. An inhibit is then produced which keeps the program from being interrupted until another TIO is received. A signal which requests an interruption in the program is then sent to the computer. The program is interrupted when the computer is bringing up the next instruction word; however, the program is not interrupted if the computer is in the Repeat mode.

As soon as the interrupt is accepted, the contents of the JA Register, including F-bit, are transferred to the left address portion of M + 2, and the contents of the PA Register are then transferred to the JA Register. Therefore, at the beginning of the executive routine, the contents of the JA Register are contained in the left address portion of M + 2, and the original contents of the PA Register are contained in the JA Register. A jump is then made to the left half of the memory location at address M + 3, and the first instruction of the executive routine is performed.

SPECIAL INSTRUCTIONS USED WITH THE AUTO-CONTROL UNIT

Two special jump instructions which are employed only with the ACU have been added to the list of Philco 2000 instructions. These instructions cause a jump to be performed without affecting the JA Register. The mnemonic code of the two jump instructions is JR (jump right) and JL (jump left), and the quaternary codes are 2320 and 0320, respectively.

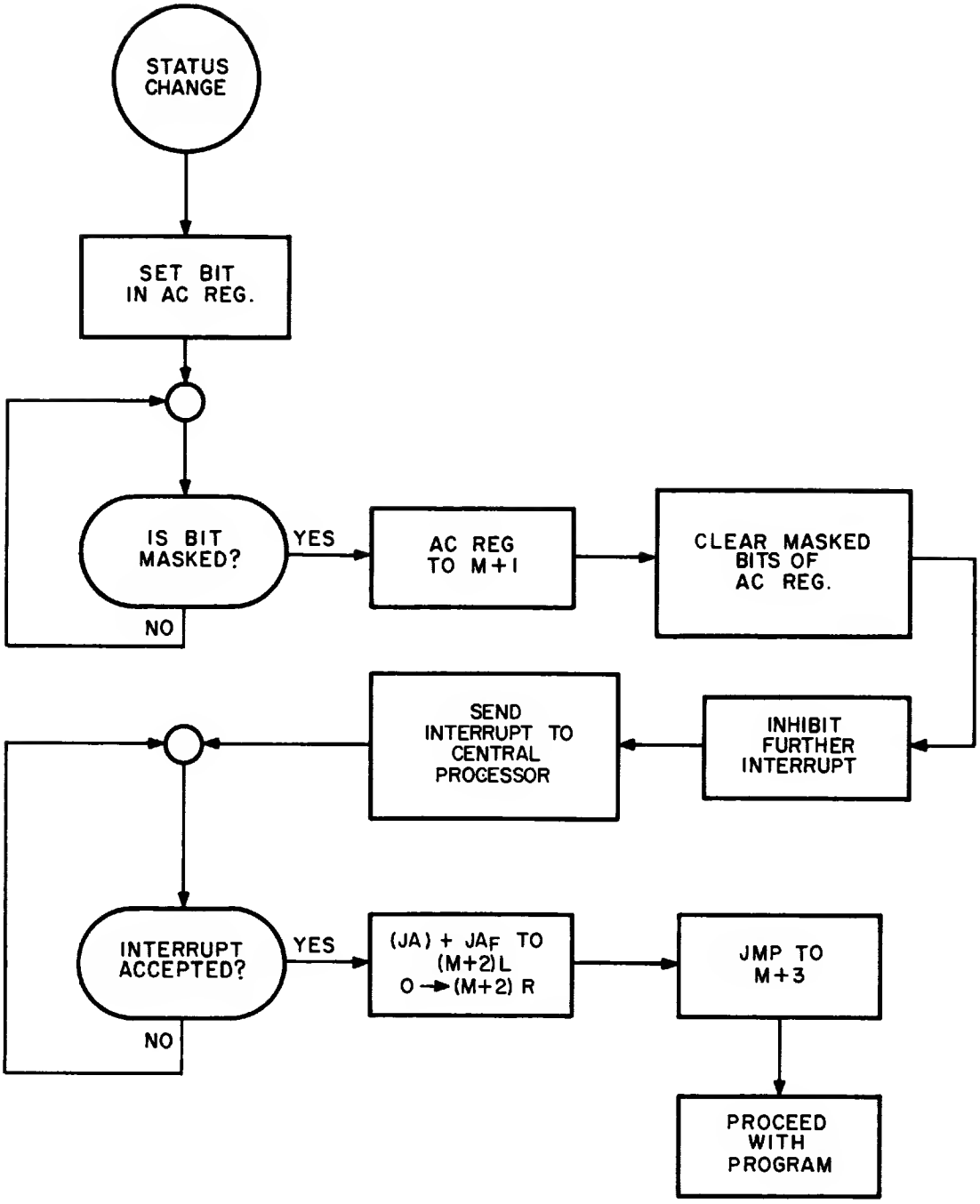


Figure RT-4. Auto-Control Operation

These instructions are normally used at the conclusion of the executive routine when the contents of all registers are restored to their original value (i. e., the value at the start of the interrupt), and when it is desired to return to the main program without affecting the contents of any registers. These instructions are accepted by TAC, and, if these instructions are used in a system that does not have an Auto-Control Unit, a command fault will occur.

Auto-Control Interrupt Conditions

The following conditions are some of those which are in use at various installations to interrupt the computer via the Auto-Control Unit. The specific bit assignments for these conditions may vary between installations.

Assembler Complete
I-O Errors
Console Interrupt
Interval Timer
UBC Complete
UBC Error
Punched Card Ready
Paper Tape Ready
All Assemblers Free

FUNCTIONAL DESCRIPTION OF THE TIMER (See figure RT-5.)

To set the Timer, a real-time output order is issued to the Timer upon the execution of a TIO instruction. The 25 low-order bits of the memory location specified in the ADDRESS field of the TIO instruction are transferred to the 25-bit register of the Timer. If the quantity in the 25 low-order bits of the specified memory location is not zero, the Timer decrements the quantity to zero and then generates a signal which indicates that the time period has elapsed. If the quantity in the specified memory location is zero, zero is set in the Timer Register, the Timer is de-activated and no signal is generated.

To obtain a readout from the Timer, a real-time input order is issued to the Timer upon the execution of a TIO instruction. Acceptance of this instruction causes the contents of the Timer Register to be transferred to the 25 low-order bits of the location specified by the ADDRESS field of the TIO instruction. The 23 high-order bits of that location are cleared to zero. (See figure RT-6.)

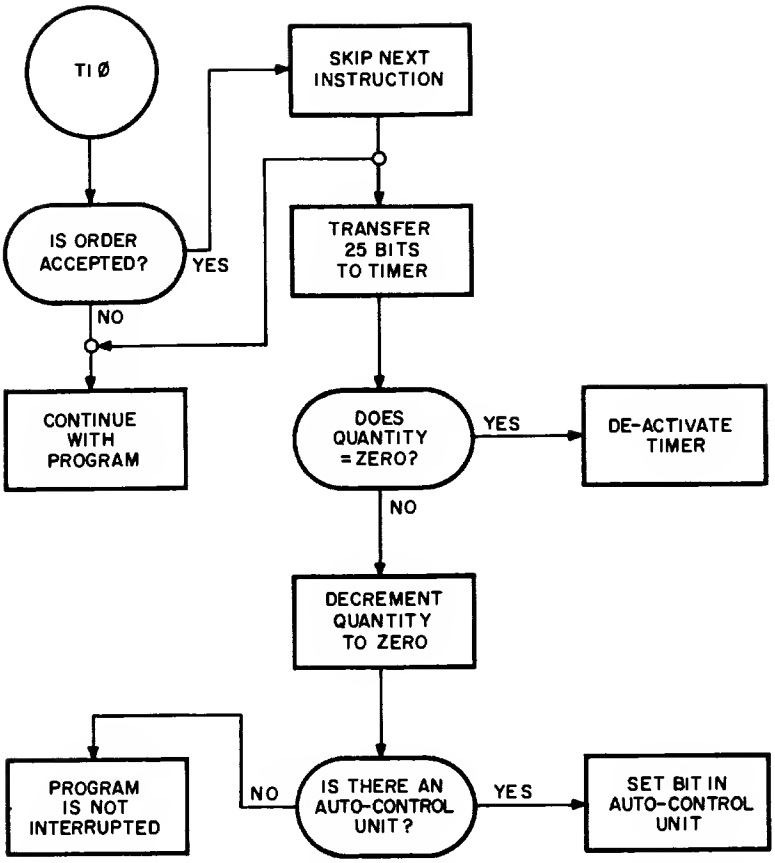


Figure RT-5. Flowchart of Output Order for Interval Timer Unit

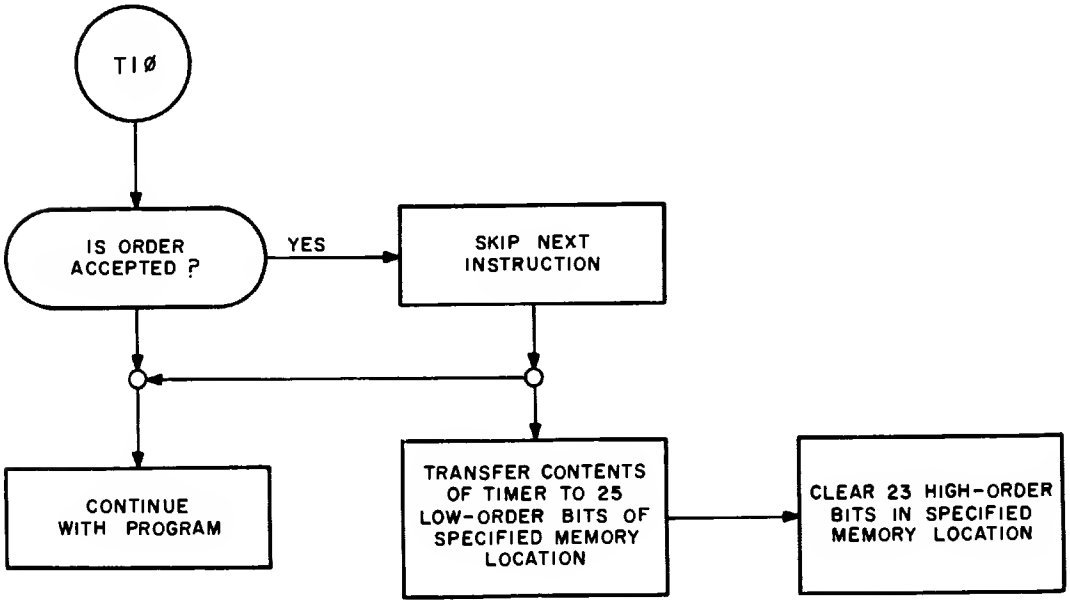


Figure RT-6. Flowchart of Input Order for Interval Timer Unit

DESCRIPTION OF INPUT-OUTPUT ORDERS AND INSTRUCTIONS

INTRODUCTION

In the preceding chapters, a functional description of each of the Philco 2000 input-output systems, their order acceptance procedure, and their tie-in with the Central Computer was presented. In this chapter, the programming methods used to initiate and to check input-output operations are outlined, and the applicable input-output orders for each system are described.

RELATION OF I-O ORDERS TIϕ AND SKIP INSTRUCTIONS

Data transmissions between the Central Computer and the input-output (I-O) systems are achieved and verified with I-O orders and with the TIO and Skip instructions. The TIO is the computer instruction which is used to transfer program control from the computer to an I-O system; the I-O order is the control information pertinent to the data transmission; and the Skip instruction is used to verify that transmission. These instructions and orders were presented in the introductory chapter, and are explained in detail on the following pages.

Before data can be transferred, control information must be made available to both the Central Computer and the desired I-O systems. This control information, for example, may specify the direction of data transmission (to or from the I-O system), the amount of information to be transferred, the I-O system involved in the transmission, etc. This information is represented in the I-O order, and these orders are written as full 48-bit computer words.

A list of all I-O orders for the Philco 2000 System is summarized on form 12-D (figure TAC - 1), which also illustrates how the D Register is apportioned into the various fields necessary to contain control information or the parameters of an I-O order.

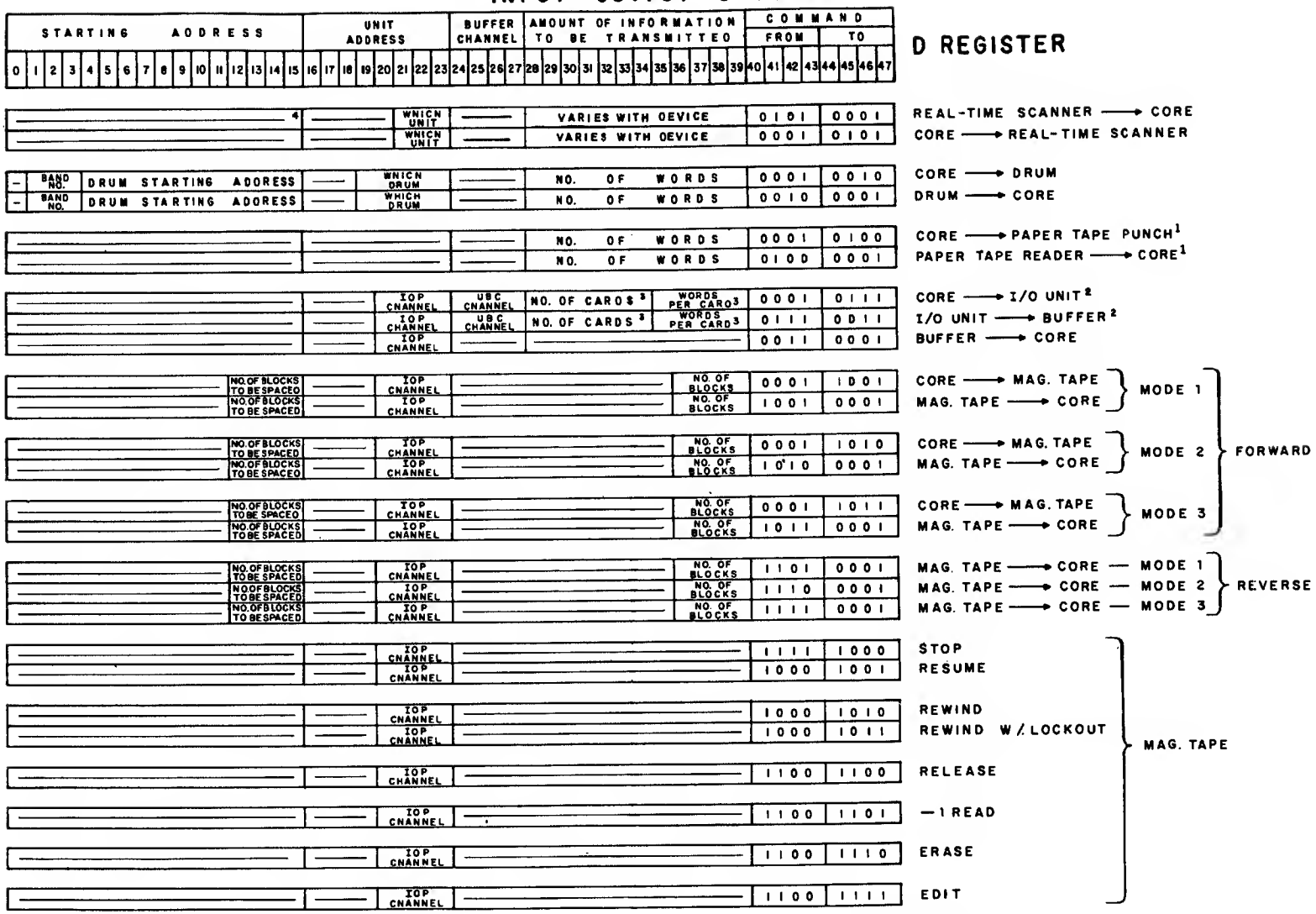
CODING INPUT-OUTPUT ORDERS

Input-Output Orders are usually written as either pool or non-pool constants. For example, a Read Forward, Mode 1 magnetic tape order (see figure TAC - 1) to space one block and read 10 blocks from Tape Unit 3, into memory locations starting with 1000_8 could be written as follows:

as a non-pool constant

LOCATION	COMMAND	ADDRESS AND REMARKS
	TMD	READ
	TIϕ	M/1000
	.	
	.	
	.	
READ	N/1T15; N/3T23; N/10T39; H/91T47	

INPUT-OUTPUT ORDERS



FUNDAMENTAL CODES

0101 REAL-TIME SCANNERS
0001 MAGNETIC CORE
0010 MAGNETIC DRUM
0011 UNIVERSAL BUFFER-CONTROLLER
0100 PAPER TAPE[1]
0101 (NOT USED)
0110 (NOT USED)
0111 I/O UNIT[2]

1000 THRU 1111 INCLUSIVE ARE USED FOR MAG. TAPE.

NOTES

1. CODE 0100 IS USED IN INSTALLATIONS WHERE THESE UNITS DO NOT OPERATE THROUGH A UNIVERSAL BUFFER-CONTROLLER.
2. CODE 0111 IS USED FOR ANY UNIT OPERATING THROUGH A UNIVERSAL BUFFER-CONTROLLER.
3. THESE BITS ARE USED ONLY WHEN THE I/O UNIT SPECIFIED IS A PUNCHED-CARD SYSTEM.
4. UNUSED FIELDS ARE INDICATED BY A LINE IN PLACE OF A LEGEND.

TF 12-D

Figure TAC-1. Input-Output Orders

as a pool constant

LOCATION	COMMAND	ADDRESS AND REMARKS
	TMD	N/1T15; N/3T23; N/10T39; H/91T47
	TIϕ	M/1000
	.	
	.	
	.	

TIϕ INSTRUCTION

The TIϕ instruction (transfer control to input-output) is an indexable instruction used to initiate the I-O order. This instruction causes the pertinent fields of the I-O order in the D Register to be transferred to the controller of the appropriate I-O system.

Coding TIϕ Instructions.

The TIϕ instruction is written immediately following the TMD instruction, which moves the I-O order from memory into the D Register. The address portion of the TIϕ instruction contains the starting address in memory for the transfer operation. If the starting location in memory were $(1000)_8$, for example, it could be written as follows:

COMMAND	ADDRESS AND REMARKS
TMD	READ
TIϕ	M/1000

Since the TIO instruction is indexable, it is possible to modify the starting address by using index registers. In this case, the starting address could appear as follows:

COMMAND	ADDRESS AND REMARKS
TMD	READ
TIϕ	0, 1X

In this example, the starting address in memory is modified by the contents of Index Register Number 1.

It is not always necessary, however, to specify a core starting address. Certain magnetic tape orders such as the Release, Stop, Resume, etc., do not require an address because they are concerned with interrupted read or write orders. In a Stop order, for example, the address portion of the TIO instruction would be left blank, and would appear as follows:

COMMAND	ADDRESS AND REMARKS
TMD	STOP
TIØ	

Action of the TIO Instruction

The action of the TIØ instruction is shown in figure TAC-2. The address part of the instruction, when included, is transferred into the I-O/MA Register of the computer. If the S bit of the instruction is a 1, the address is added to the contents of the specified index register before being transferred into the I-O/MA Register. If the S bit is 0, the address is transferred unchanged.

The command portion of the I-O order in the D Register is then decoded and the I-O system specified by that code combination is interrogated to determine whether or not the order can be accepted. If the order can be accepted, the computer transfers the contents of the D and I-O/MA Registers to the specified I-O system, skips the next sequential program instruction and proceeds with the remaining instructions in the program. If the order is not accepted, or if the command is illegal, the computer executes the next sequential program instruction. At this point, skip instructions may be used to determine the specific condition which prevented the acceptance of the order. (In most cases, the instruction following the TIO is a jump to a diagnostic routine which contains a series of skip instructions.) A detailed description of skip instructions is presented later in this chapter.

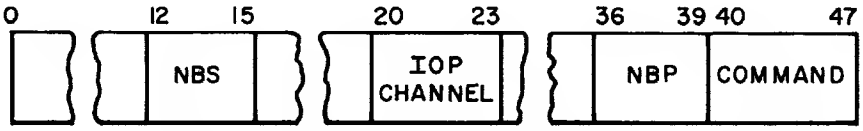
DESCRIPTION OF INPUT-OUTPUT ORDERS

Basically, there are three classes of input-output orders; those involving magnetic tape units connected to the IOP, those involving devices connected to the UBC, and those involving devices connected directly to the IOB.

MAGNETIC TAPE ORDERS

The magnetic tape orders can be divided into read and write orders, orders that concern read and write orders which have been interrupted, and orders that rewind and edit magnetic tape.

There are nine different read and write orders, and their general format is shown below:



NBS is the number of blocks to be spaced. It can be written numerically 0 to 15. The NBS is placed in the NBS Register of the assigned assembler in the IOP and is reduced by one for each block spaced.

IOP CHANNEL is the channel to which the desired magnetic tape unit is connected.

NBP is the number of blocks to be processed. It may be specified numerically from 0 to 15. The NBP is placed in the NBP Register of the assigned assembler in the IOP and is reduced by one for each block processed. If both the NBS and NBP fields are specified as zero, the order is interpreted to process 16 blocks.

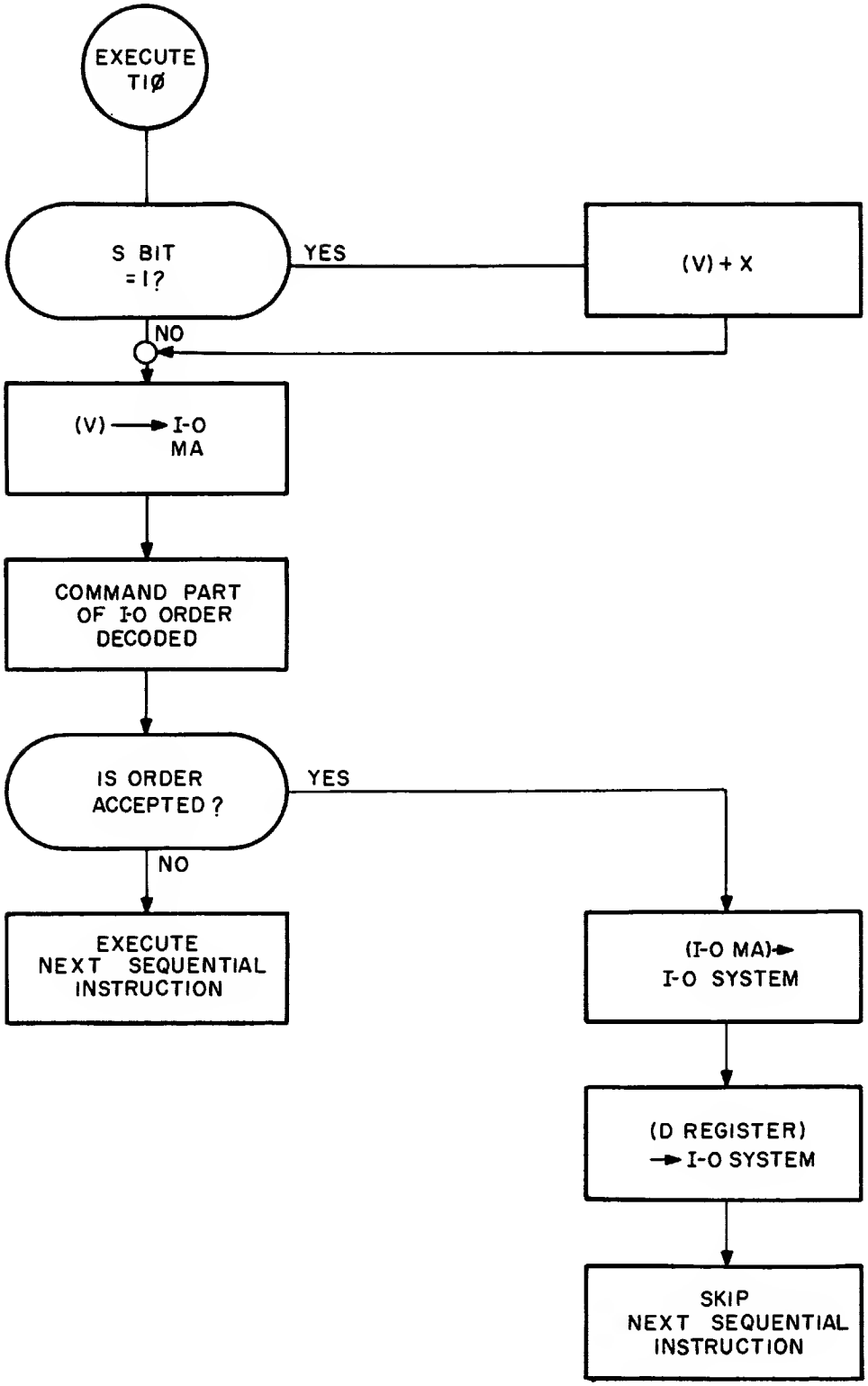


Figure TAC-2. Flowchart of TIO Instruction

COMMAND is the operation to be performed.

The Read Order

The Read order causes the number of blocks specified by the NBS field to be spaced and the number of blocks specified by the NBP field to be processed from the tape unit specified by the IOP CHANNEL field. The first memory location to be accessed by the order is designated by the address portion of the TIO instruction.

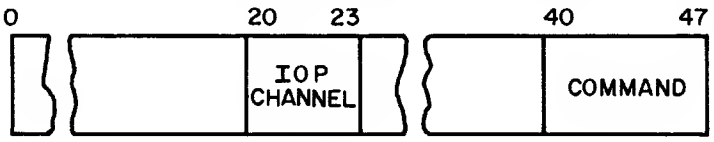
Before processing begins, the Run and Busy Registers in the assigned assembler are set to one, and the Parity, Space, and Sprocket error indicators are cleared. A flow chart showing the action of the order is contained in figure TAC-3.

The Write Order

The Write Order causes the number of blocks specified by the NBS field to be spaced and the number of blocks specified by the NBP field to be processed from the tape unit specified by the IOP CHANNEL field. The first memory location to be accessed by the order is designated by the address portion of the TIO instruction.

Before processing begins, the Run and Busy Registers in the assigned assembler are set to one, and the Parity, Space, and Sprocket error indicators are cleared. A flow chart showing the action of the order is contained in the figure TAC-4.

The general format of the remaining eight magnetic tape orders (Stop, Release, -1 Read, Erase, Resume, Rewind, Rewind with Lockout, and Edit) is shown below:



IOP CHANNEL is the channel of the IOP to which the desired magnetic tape unit is connected.

COMMAND is the operation to be performed.

The Stop Order

The Stop order causes memory accessing to stop, any error indicators other than space, parity or sprocket, to be cleared and the assigned assembler to be released. The order may be issued while the tape is in motion and is accepted regardless of any error conditions that may be present.

Following the acceptance of the Stop order, core storage accessing stops, and the previous order is terminated at the end of the current block being processed. If an error cycle is being performed, the original read or write order is terminated at the beginning or end of the block being backspaced or erased, whichever block mark is reached first. The position of the read/write heads, therefore, is questionable following stop orders. That is, the read/write heads may be either at the beginning or end of the last block processed.

Termination while backspacing may also occur if a Stop order is executed during the performance of the -1 Read or Erase orders. The Stop order, however, does not terminate

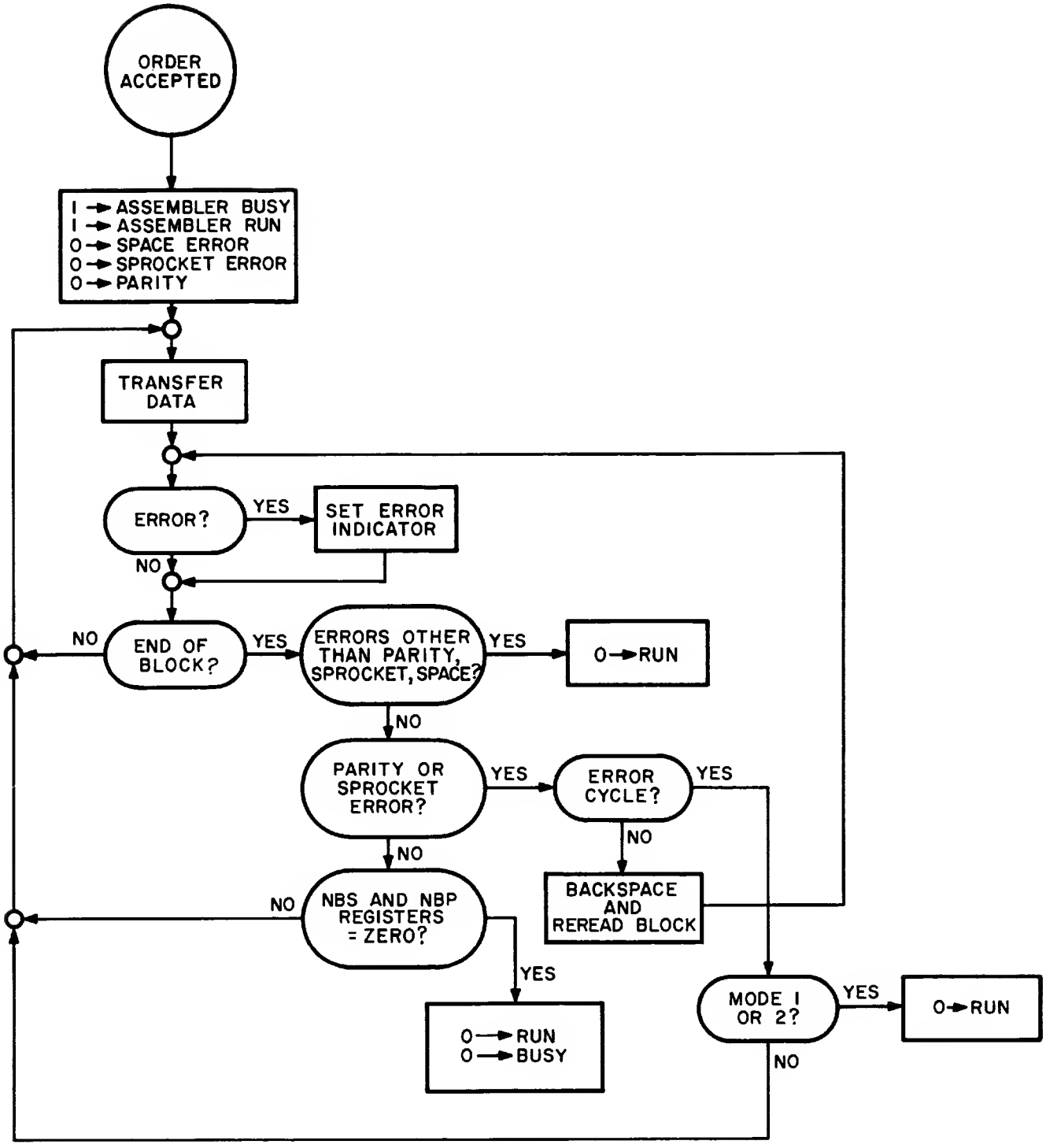


Figure TAC-3. Flowchart of Magnetic Tape Read Order

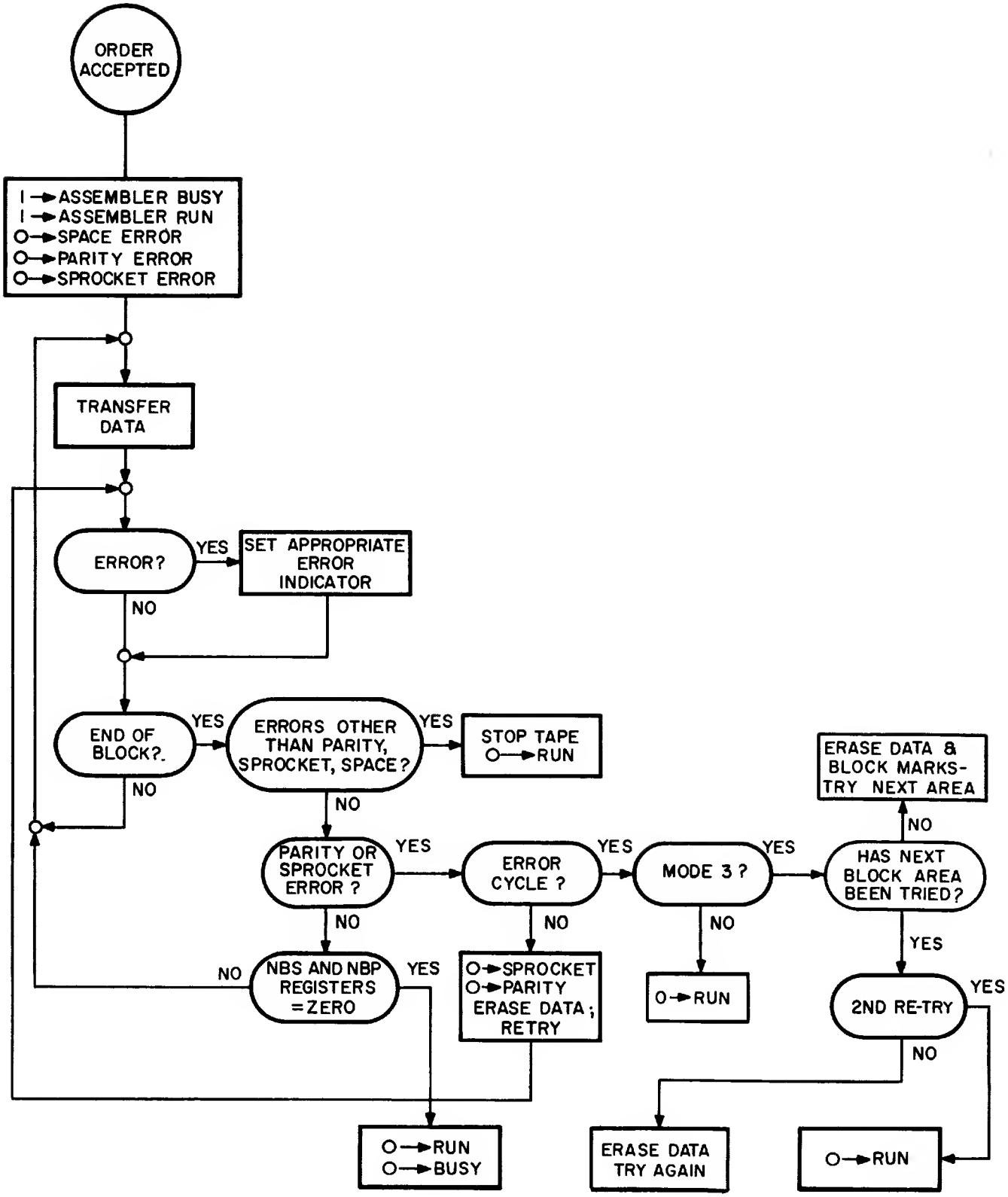


Figure TAC-4. Flowchart of Magnetic Tape Write Order

a previous order until the NBS equals zero. A primary function of the Stop order is to terminate memory accessing. Spacing, which does not require memory accessed, need not be terminated. A flow chart showing the action of the order is contained in figure TAC-5.

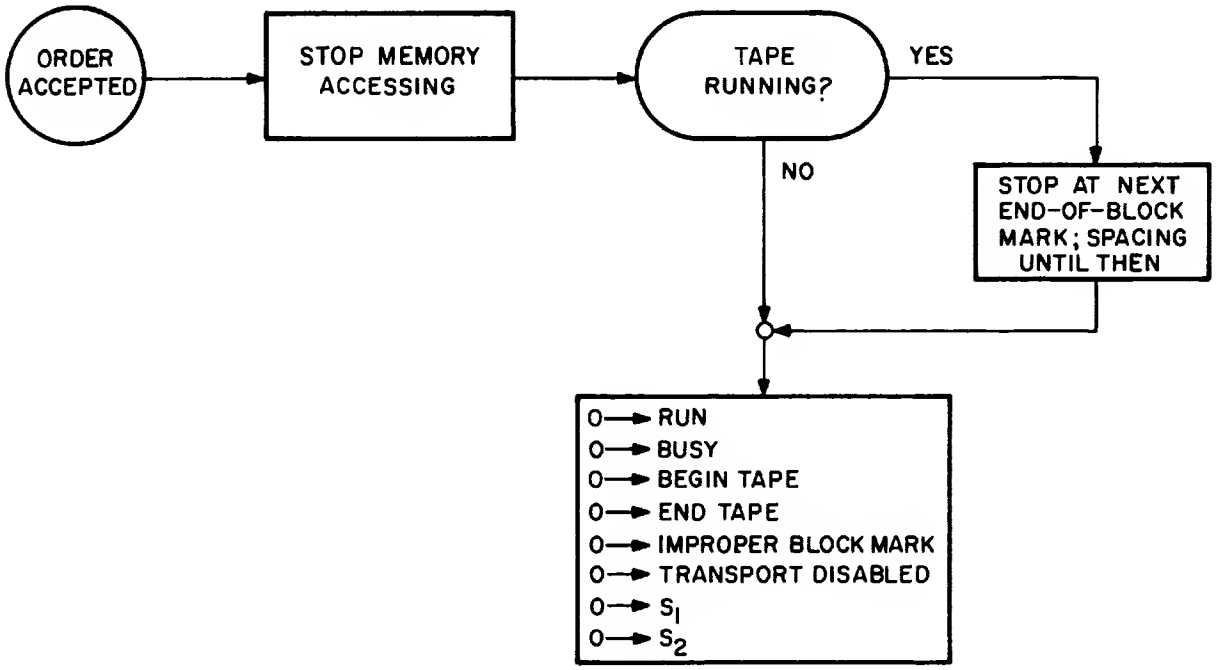


Figure TAC-5. Flowchart of Magnetic Tape Stop Order

The Release Order

The Release order causes the assigned assembler to be released from the operation at the next convenient point. That is, the operation stops and the assembler is released when the current block is processed, including any error cycle which may be in progress.

No error indicators are cleared by the Release order, and, if any error condition other than a parity, sprocket, or space error occurs before the Release order is completed, the assembler is not released.

If the Release order is executed during the backspace phase of a -1 Read or the Erase order, termination will not occur until that order is completed. Like the Stop order, the Release order will not terminate an operation until the NBS equals zero. A flow chart showing the action of the order is contained in figure TAC-6.

The -1 Read Order

The -1 Read order may be used following Read, but not Write, orders which have been interrupted by a parity error. The -1 Read order will not be accepted if the tape is in motion when the order is executed.

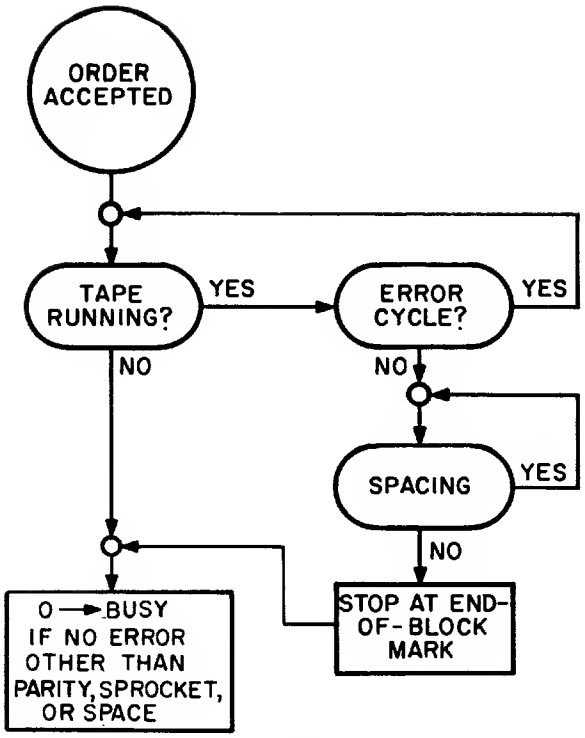


Figure TAC-6. Flowchart of Magnetic Tape Release Order

Execution of this order causes the last block which was read to be reread in the same direction as the original read, and into the same memory locations. However, any word containing a parity error on the reread is not placed in memory. Instead, the number -1 (1 and 47 zeros) is placed in that memory location. This operation will destroy any valid data appearing in the possible three good frames of the four which form a 48-bit word. The core address at the termination of the order is the same as before the order was issued.

Upon completion of the order, the tape is in the same position relative to the read/write heads as it was when the order was executed. The parity and sprocket error indicators are cleared, and the assembler remains connected. The original Read order may be resumed by the execution of a Resume order after the -1 Read order has been completed. A flow chart showing the action of the order is contained in figure TAC-7.

The Erase Order

The Erase order is used to remove a block of data, (including sprocket and block marks) from a tape in locations where information cannot be written in modes 1 or 2. The order will not be accepted if the tape is in motion or if the write ring is not mounted on the tape reel.

In operation, the order causes the tape to backspace over the last block to pass under the read/write heads, then erases the block. Successive blocks may be erased by the issuance of successive Erase orders. The Erase order is terminated with the assigned assembler connected and with the Parity, Sprocket, and any Block Mark error indicators

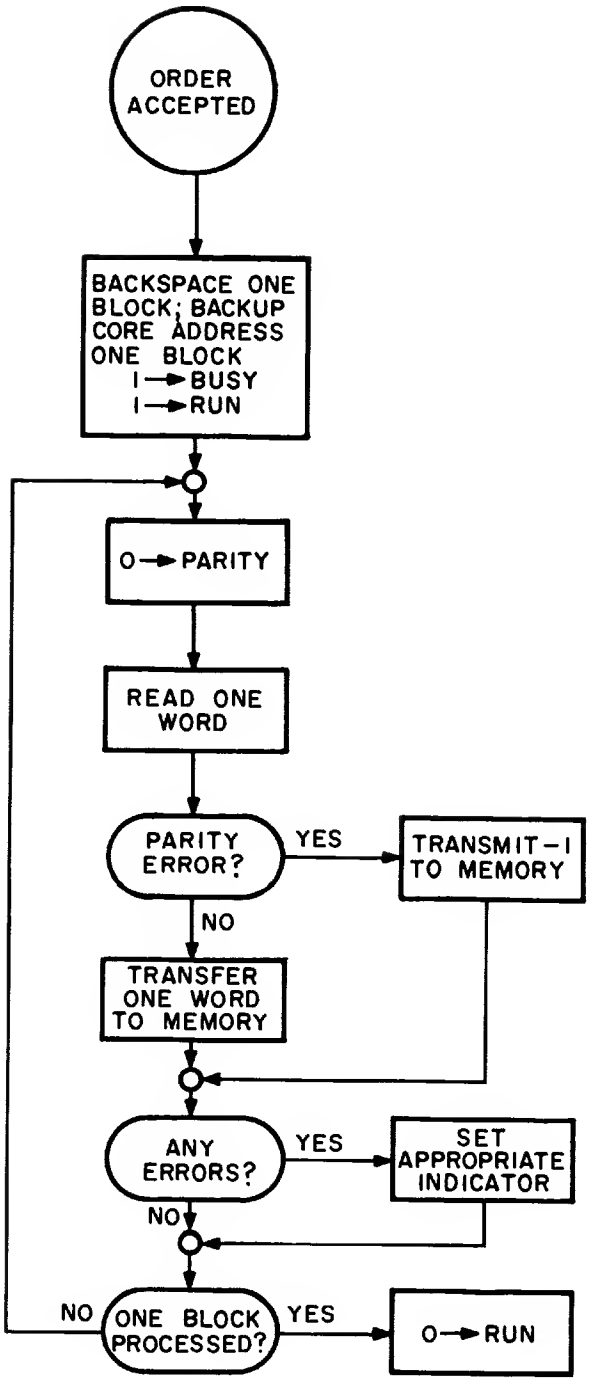


Figure TAC-7. Flowchart of Magnetic Tape -1 Read Order

cleared. Neither the NBP nor the memory access counter registers are disturbed by this order. A flow chart showing the action of the order is contained in figure 61.

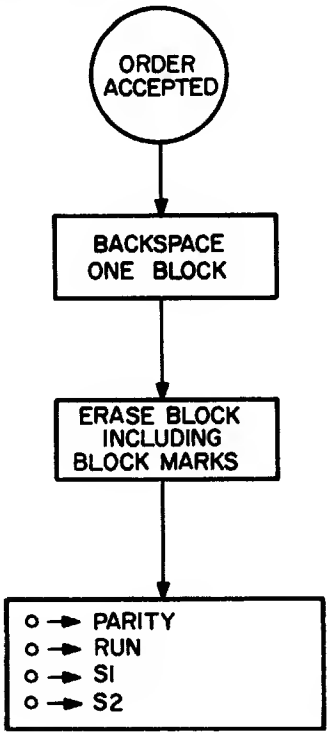


Figure TAC-8. Flowchart of Magnetic Tape Erase Order

The Resume Order

The purpose of the Resume order is to permit the completion of a Read or Write order which was interrupted by a parity or sprocket error. The order may be given after an Erase, a -1 Read, or immediately following an error cycle halt. The operation of the Resume order differs depending on whether the previous order was a Read or a Write. In both cases, however, the Parity and Sprocket error indicators are cleared when the order is accepted.

Following a Mode 1 or 2 Read order, the Resume order simply initiates the operation from the point where it was terminated. In effect, a Resume order executed following a Mode 1 or 2 Read order is the same as a Mode 3 Read order. For example, if a Mode 1 Read order to process five blocks were executed, and if a parity error occurred when the second block was processed which was not eliminated by rereading that block, the order would be terminated. If the Resume order were given, and no further error conditions resulted, data would be read into core memory as follows.

Locations L through L + 127 would contain the first block.
Locations L + 128 through L + 255 would contain the second block. (in error)

} Read by the original Order

Locations L + 256 through L + 383 would contain the third block.
Locations L + 384 through L + 511 would contain the fourth block.
Locations L + 512 through L + 639 would contain the fifth block.

} Read by the Resume Order

If a -1 Read order had been given prior to the Resume order, the same core memory format would have resulted except that any words in the second block which contained parity errors would have been replaced in memory by -1.

Following a Mode 1 or 2 Write order, the Resume order initiates rewriting of the block of information which could not be written by the original order. This attempted rewrite is in the next sequential block to the one which was erroneously written. For example, if a Mode 1 Write order to process five blocks were executed, and if a parity error occurred when the second block was processed which was not eliminated by rewriting that block, the order would be terminated. If the Resume order were given, and no further error resulted, data would be written from the following core memory locations.

The first block would contain locations L through L + 127.

The second block would contain locations L + 128 through L + 255. (improperly written)

The third block would contain locations L + 128 through L + 255. (correctly written)

The fourth block would contain locations L + 256 through L + 383.

The fifth block would contain locations L + 384 through L + 511.

The sixth block would contain locations L + 512 through L + 639.

If an Erase order had been executed preceding the Resume order, the second block would have been erased, and there would not have been repetition of written blocks, (i.e., blocks 2 and 3 would be the same).

When the Resume order is given following a Read, a Space Only Read, or a Write order in which the NBP count is zero, an additional 16 blocks will be automatically processed, starting from the next sequential memory location after that filled by the original order.

In the case where a Write order has been terminated by a sprocket or parity error in the last block to be written (i.e., the NBP count has been reduced to zero), the Resume order causes the last block to be written again. A flow chart showing the action of the Resume order is contained in figure TAC-9.

The Rewind and Rewind With Lockout Orders

Rewinding of a tape may be performed by a Rewind or Rewind With Lockout order. These orders cause a tape to be rewound until the metallic begin tape leader is sensed. The lockout option places the tape transport in local status upon acceptance of the order, and causes the REWIND LOCKOUT indicator to light. Both the REWIND LOCKOUT and LOCAL buttons must be depressed (not simultaneously) to remove the transport from LOCAL status.

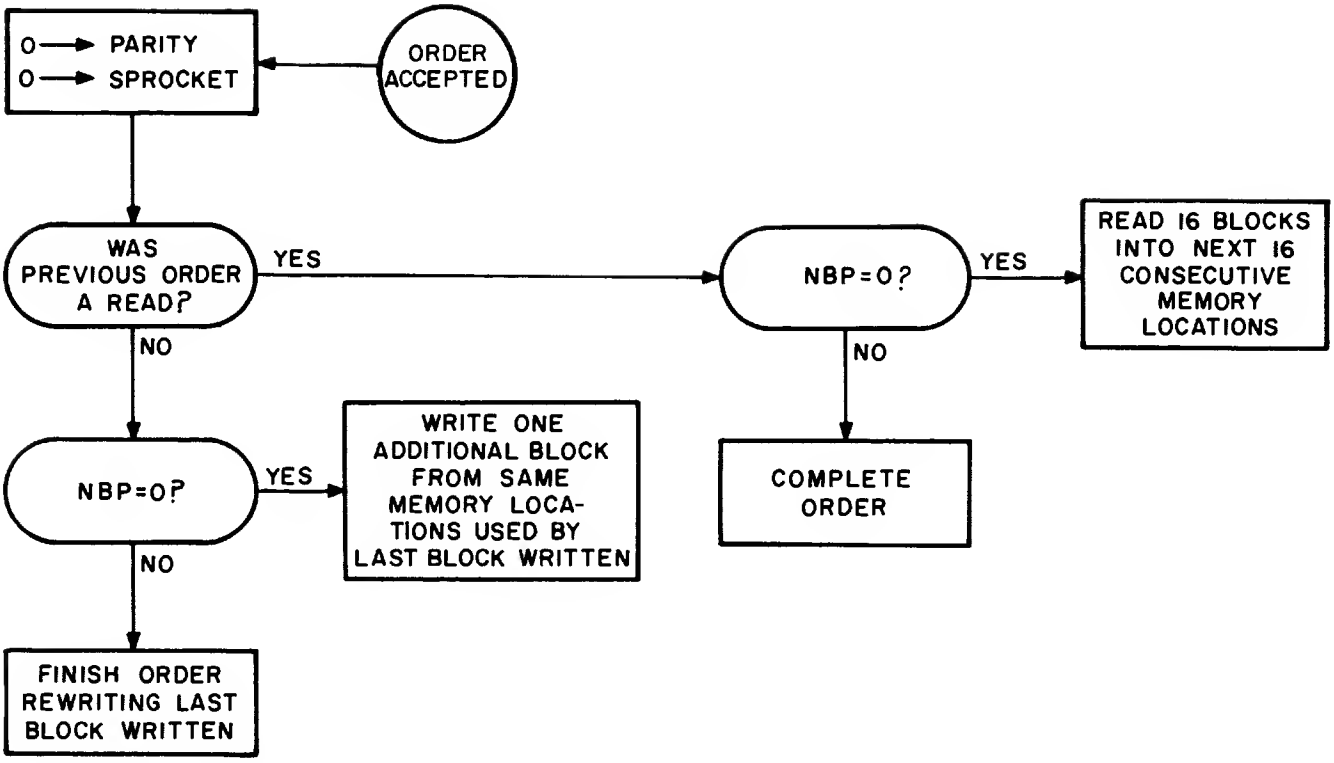


Figure TAC-9. Flowchart of Magnetic Tape Resume Order

If a Rewind order is issued to a transport which is already rewound, the order is accepted, but no tape motion occurs.

The Rewind order does not require the use of an assembler; therefore, the order may be executed even though all of the assemblers are busy. Furthermore, any number of transports may be rewinding simultaneously.

The Edit Order

The Edit order erases a tape and records beginning and ending block marks over the entire reel. While the Edit order is being executed no error indicators can be set except UNIT DISABLED and END TAPE (EOT). The EOT is set when the order is completed. Upon completion of the order the assembler remains connected.

If the tape is not rewound, the Edit order will process only that portion of the tape that remains on the supply reel.

To have an Edit order executed correctly, the order requires the assignment of Assembler Number One. If that assembler is busy, the IOP will attempt to assign another non-busy assembler; hence, the programmer must make sure that Assembler Number One is assigned to the order.

The Stop and Release orders have no effect on halting the Edit order; however, upon completion of the order, they may be used to release the assigned assembler.

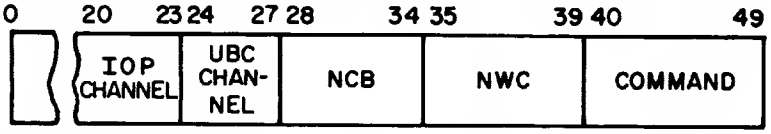
UBC INPUT-OUTPUT ORDERS

Any of the peripheral input-output systems connected to the UBC, with the exception of the magnetic tape units, may be operated on line through the UBC. Writing of a block of data

on one of the I-O systems is accomplished in one order, but reading a block of data from an I-O system required two orders. When writing, words are transferred from memory into the 128 word storage area, and then to the I-O system connected to the UBC. The assigned IOP assembler remains connected until an entire block of data has been transmitted to the UBC buffer area. The assembler is then released and is available for reassignment while the contents of the storage area are being transferred to the output system.

When reading, the 128 word storage area in the UBC is first filled from the I-O system. A second order causes the entire block in the buffer to be transferred to memory. In this manner, an IOP assembler is free to be assigned to another channel, and memory is not accessed until the full block of information has been formed in the UBC and the second I-O order is given.

The general format of the UBC Input-Output order is shown below:



IOP CHANNEL is the channel of the IOP to which the UBC is connected.

UBC CHANNEL is the channel of the UBC to which the desired I-O system is connected.

NCB is the number of cards per block (for a punched-card order only).

NWC is the number of words per card (for a punched-card order only).

COMMAND is the operation to be performed.

The UBC orders cause a one block transfer in direction specified by the command. After the order is accepted, all error indications in the Buffer Fault Register are cleared. Since all data transferred between the UBC and the computer memory must pass through the IOP, assemblers must be assigned to the operation. Therefore, the Parity, Sprocket, and Space error indicators in the assigned assembler are also cleared.

When transferring data from memory to I-O systems other than the Punched-Card System, the amount of information need not be specified. All transmissions involving the UBC automatically call for a transfer of 128 words. When the desired I-O system is punched-cards, however, the format of data being punched must be specified. During punched card operations, a NWC field and NCB field of zero will be interpreted as one word per card and 128 cards per block. If less than 128 words are designated when punching, the remaining number of words in memory (up to 128) must be filler characters. If less than 80 columns per card are designated, all remaining columns in the card will be left blank.

When transferring data from an I-O system to the UBC, the address portion of the TIO is not used; however, all other parameters must be stated. When transferring data from the UBC to memory, no UBC channel need be specified because data has already been loaded into the UBC from the I-O system. All other parameters, plus the first memory location (in the address portion of the TIO) must be stated. A flow chart of each UBC order is contained in figures TAC-10, TAC-11, and TAC-12.

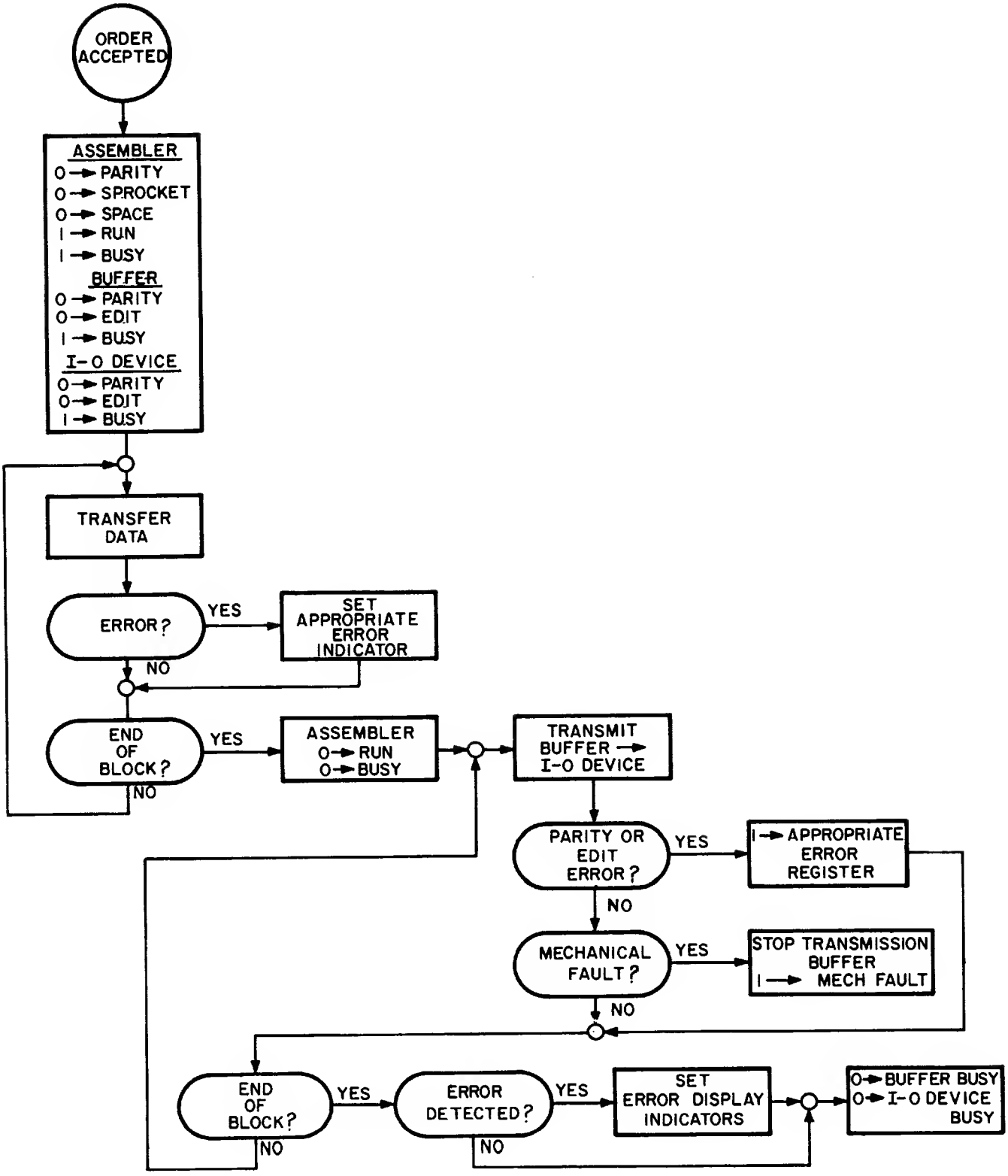


Figure TAC-10. Flowchart of I-O Order, Core to I-O Device (Through Buffer)

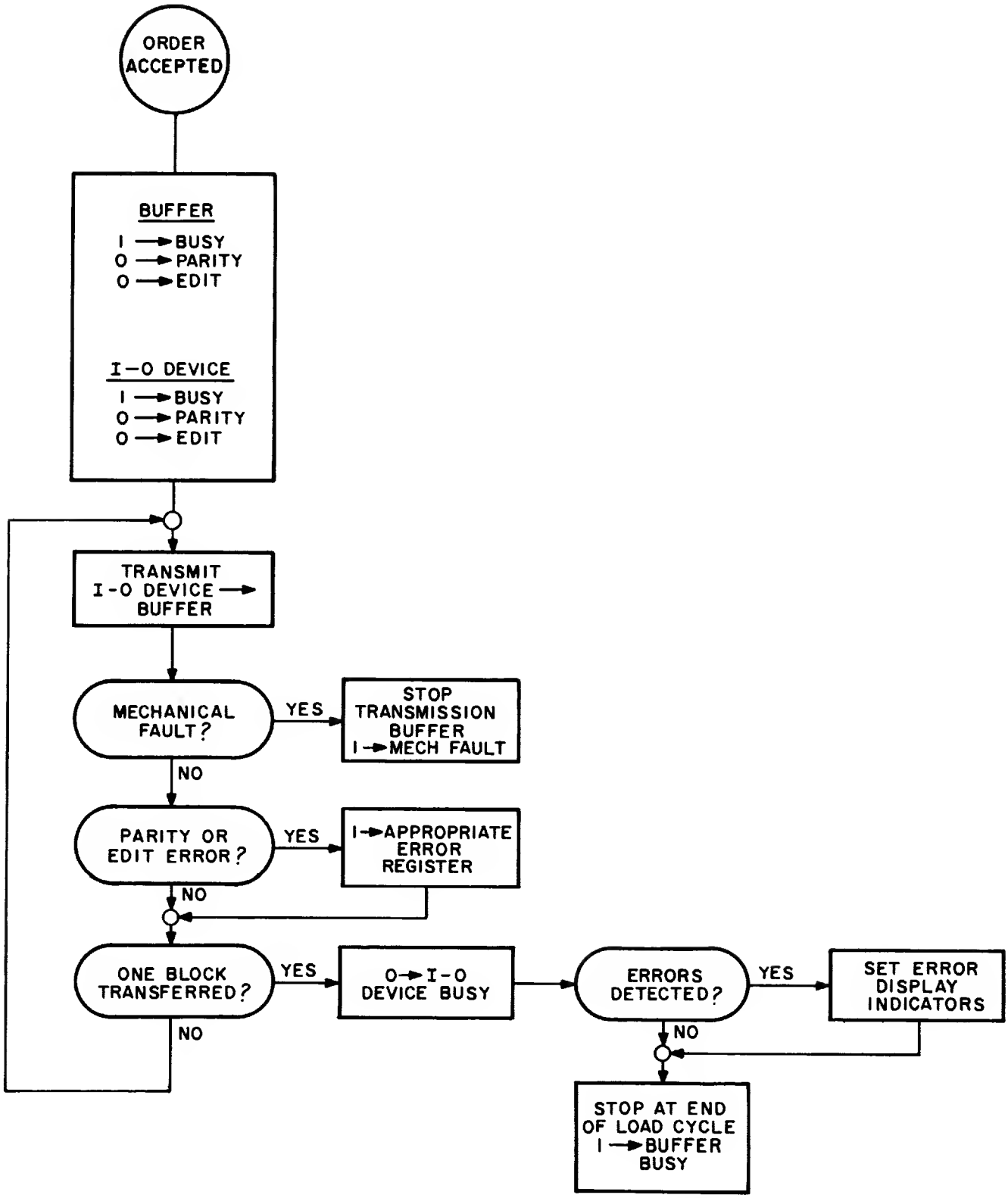


Figure TAC-11. Flowchart of I-O Order, I-O Device to Buffer (On-line Push Button on Buffer Depressed)

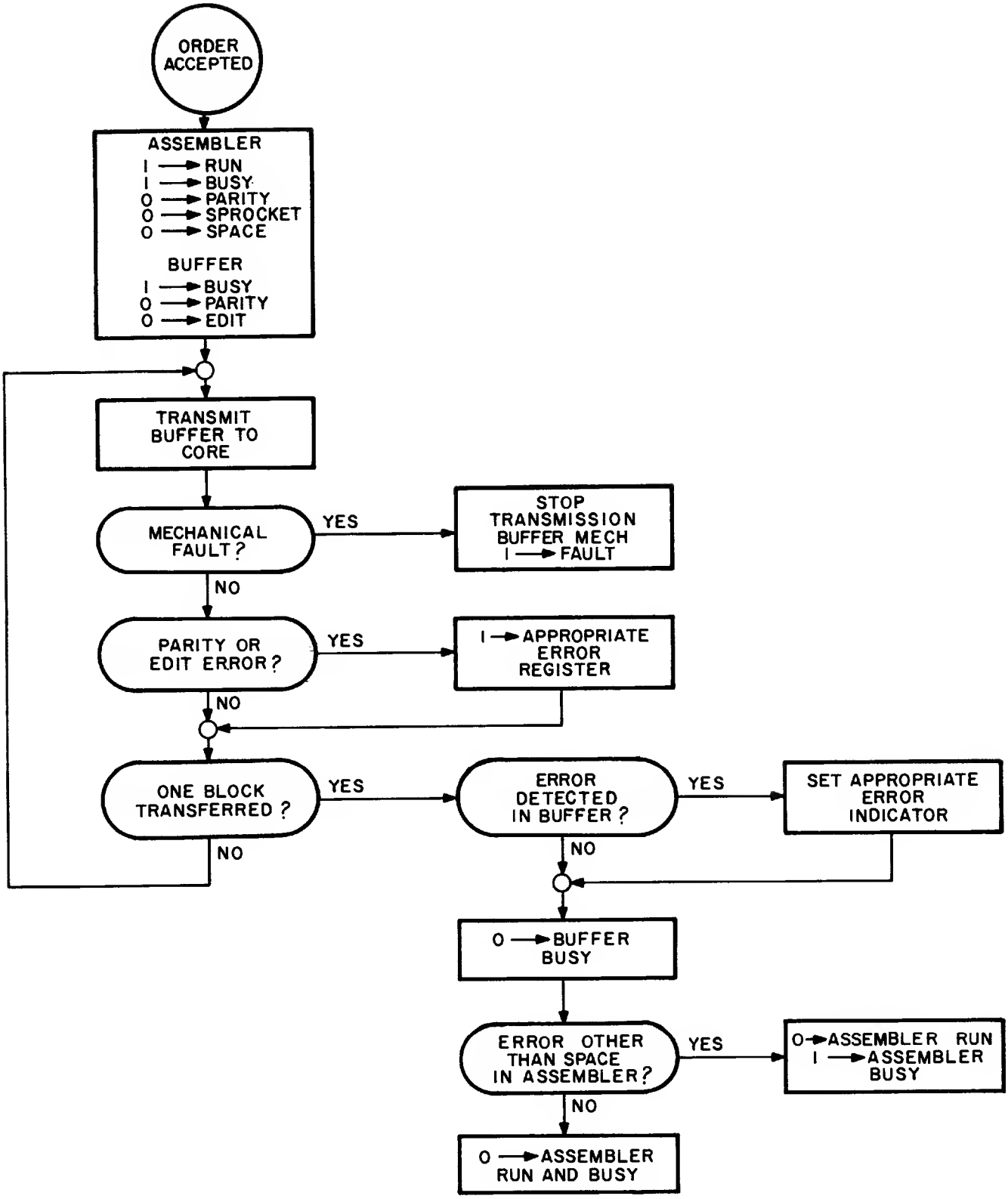
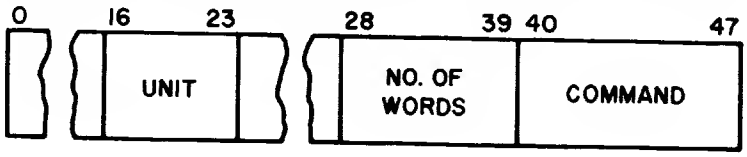


Figure TAC-12. Flowchart of On-Line I-O Order, Buffer to Core

PAPER TAPE ORDERS

The general format of the paper tape I-O order applicable to Paper Tape Systems operating through the IOB is shown below. This order can be used to initiate transmissions from either a Paper Tape System or from the Accounting Clock System.



UNIT is the designated system.

a. Binary 00000000 - Paper Tape System

b. Binary 00001000 - Accounting Clock System

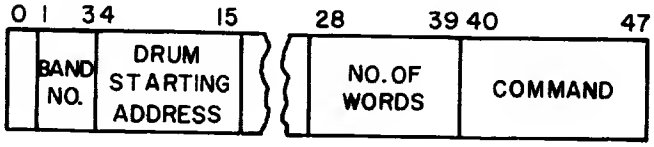
NO. OF WORDS is the number of words to be read or punched

COMMAND is the desired operation

This order causes the number of words specified by the NO. OF WORDS field to be transferred between the computer memory and the unit specified by the UNIT field. Following the acceptance of the order, the Parity error indicator is cleared and a 1 is placed in the Busy Register. Flow charts showing the action of the orders are contained in figures TAC-13 and TAC-14.

MAGNETIC DRUM ORDERS

The general format of the magnetic drum I-O order is shown below:



BAND NO. is the number of the first band to be processed; the number may be specified numerically from 0 to 7, with 0 being interpreted as 8.

DRUM STARTING ADDRESS is the location of the first word on the selected band to be processed; the number may be specified numerically from 0 to 4095, with 0 being interpreted as 4096.

NO. OF WORDS is the number of words to be processed; it may be specified numerically from 0 to 4095, with 0 being interpreted as 4096.

The magnetic drum I-O order causes the transfer of the number of words specified by the NO. OF WORDS field, and starting at the location specified by the BAND, and ADDRESS fields. After the order is accepted, the Drum Address Fault and the Read Amplifier Fault indicators are cleared, and a 1 is placed in the Busy Register. Flowcharts showing the actions of the orders are contained in figures TAC-15 and TAC-16.

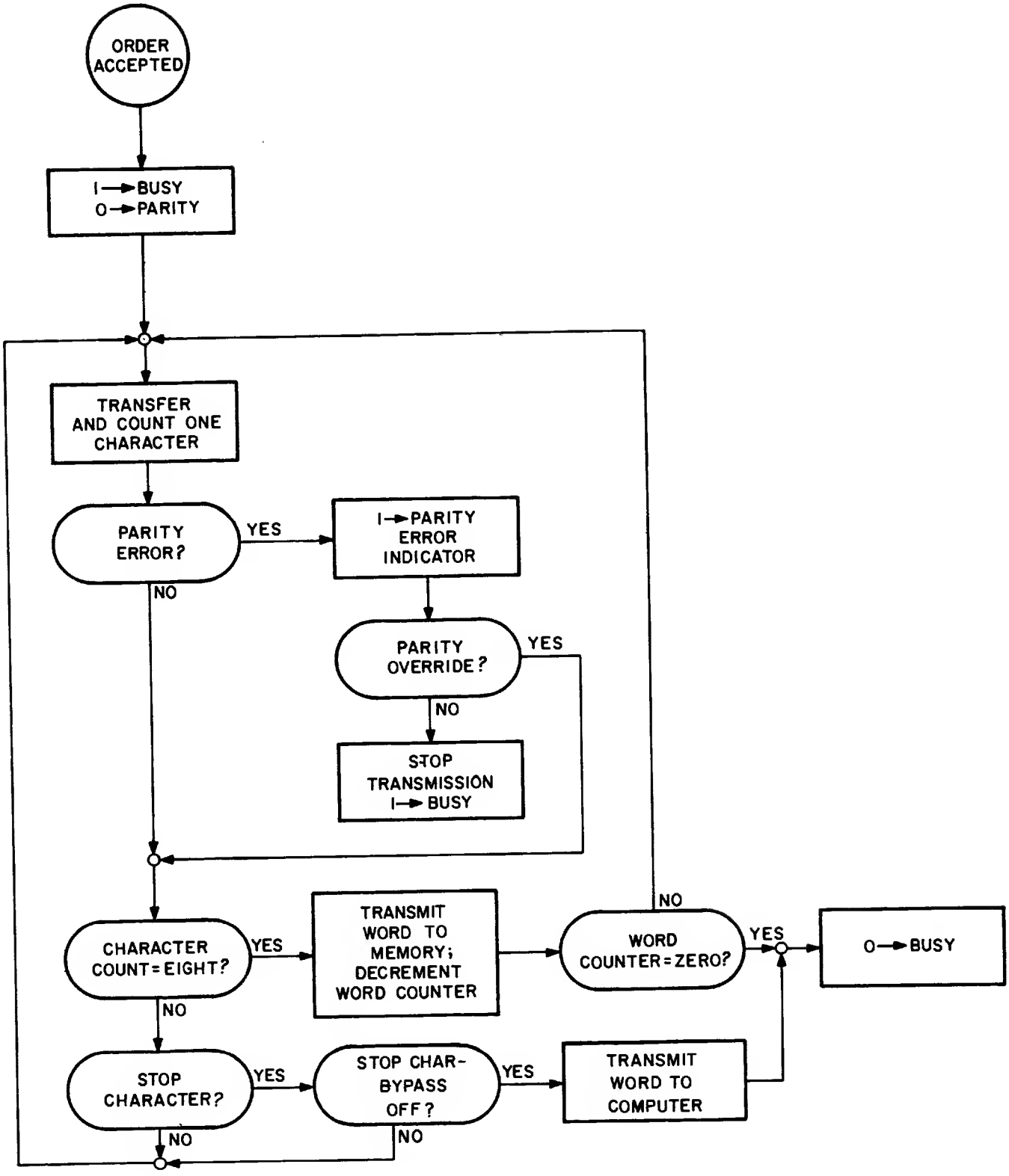


Figure TAC-13. Flowchart of I-O Order, Paper Tape to Core (Not Through IOP)

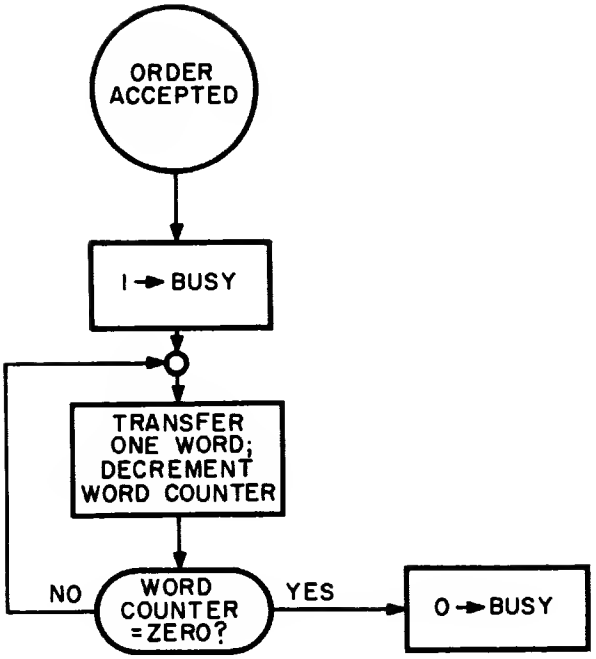


Figure TAC-14. Flowchart of I-O Order, Core to Paper Tape (Not Through IOP)

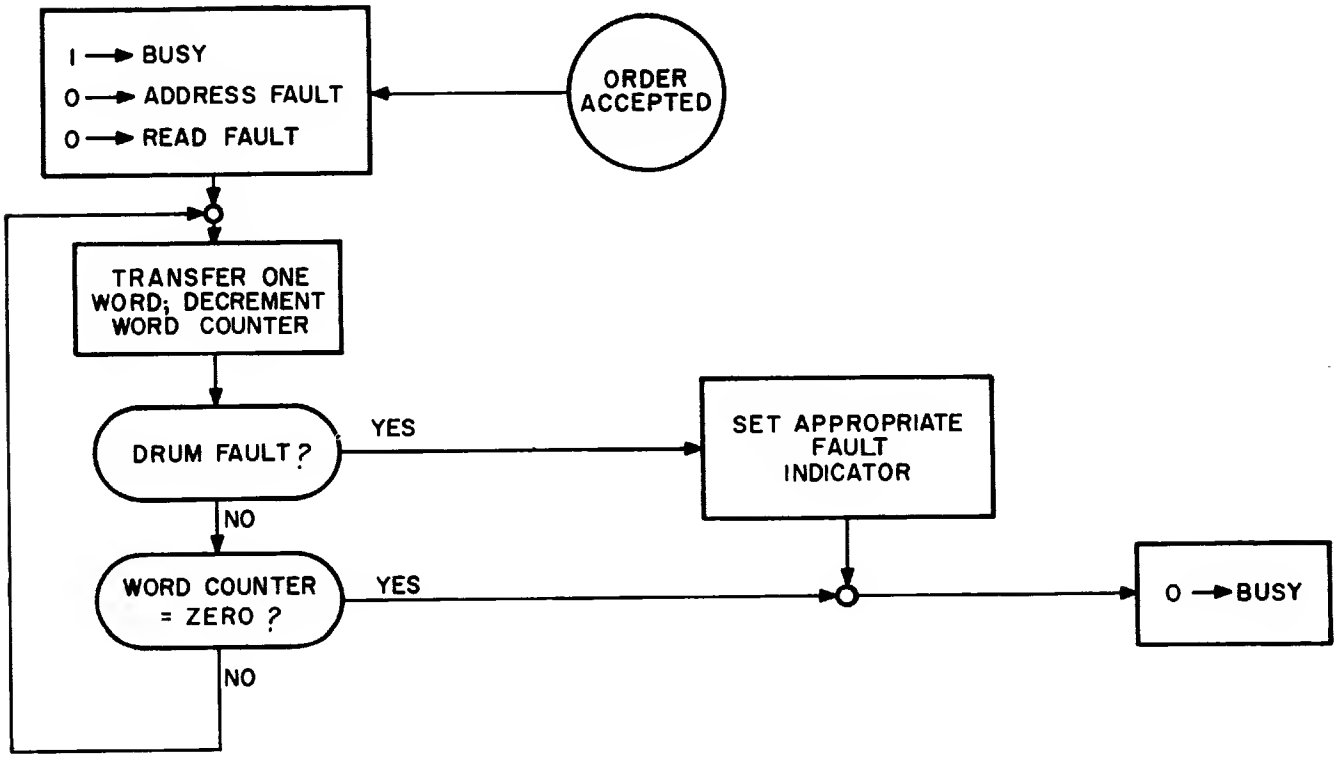


Figure TAC-15. Flowchart of I-O Order, Drum to Core

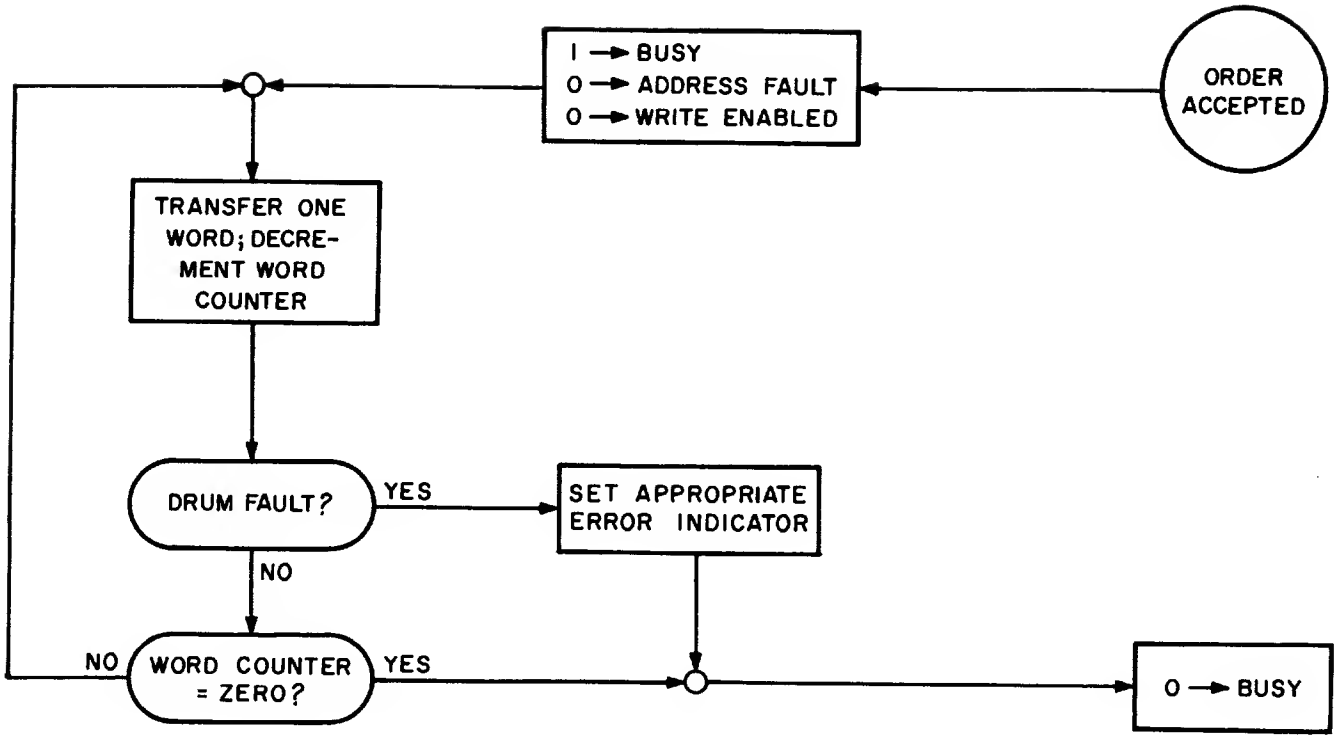
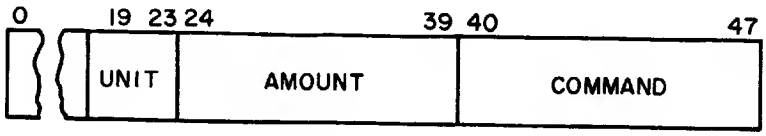


Figure TAC-16. Flowchart of I-O Order, Core to Drum

REAL-TIME ORDERS

The Interval Timer and the Auto-Control Units are controlled by the real-time input-output orders, and the orders are sent to these units through the Real-Time Scanner. The general format of the real-time order is shown below:



UNIT is the number of the real-time unit and varies at each installation

AMOUNT is the amount of information to be transferred

COMMAND is the desired operation.

The Real-Time order causes the amount of data designated by the AMOUNT field to be transferred between the computer memory and the unit specified by the UNIT field. The error indicators that are cleared depend upon the specific real-time unit.

The Auto-Control Unit will accept a Read order only. In installations that do not have an Auto-Control Unit, a Write order issued to the Interval Timer will set the Timer, but the program will not be interrupted when the Timer equals zero.

SKIP INSTRUCTIONS AND RELATED INPUT-OUTPUT REGISTERS

Skip instructions provide the programmer with the means to interrogate various information registers located in the input-output systems in order to determine the status of the systems and the progress of data transmissions through them.

In the Philco 2000, two types of skip instructions are used; the Skip Check (SKC) and the Skip if no Fault (SKF) instructions. The SKC instruction is used when checking status and counter registers, and the SKF instruction is used when checking fault registers. Status registers indicate the availability of an I-O system; the counter registers indicate the amount of information remaining to be transmitted to or from an I-O system (if the processing operation has been interrupted); and fault registers indicate faults detected during transmissions.

ACTION OF SKIP INSTRUCTIONS

Checking is accomplished by comparing the contents of a designated information register of an I-O system with a field, called the Comparison Quantity field, contained in the address portion of the Skip instruction. The format of the Comparison Quantity field is determined by the programmer and depends upon the specific condition to be checked. A complete account of the possible conditions reflected by each information register is contained later in this chapter.

Both terms to be compared are considered to be numeric quantities. In operation, the Comparison Quantity (CQ) field and the contents of the register being checked are transferred into an adder network of the Central Computer. In the adder they are compared, and if the absolute value of the bit configuration in the register is greater than the absolute value of the comparison quantity, the next sequential instruction in the program is performed. If, however, the absolute value of the information register is less than or equal to the comparison quantity, the next sequential instruction in the program is skipped. Basically, skip instructions function in a manner similar to the TIO instruction; that is, a skip occurs when specified conditions exist in the operation. Otherwise, the skip will not take place. The action of the skip instruction is shown in figure TAC-17.

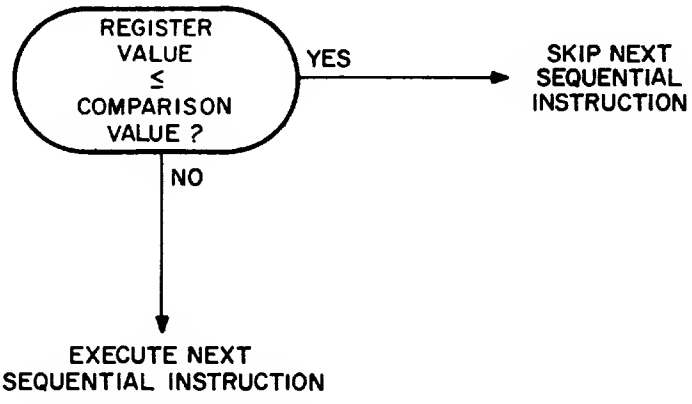


Figure TAC-17. Flowchart of Skip Instructions

FORMAT OF SKIP INSTRUCTIONS

The SKC and SKF are 24-bit instructions, and the format of both is illustrated in figure TAC-18. When the S bit (selector) is 1, it indicates that the SC field is part of the Comparison Quantity field; the SC field (sub-command) designates the register to be checked when the S bit is 0. The UNIT field specifies the IOP, Drum, or Real-Time Channel. The CQ field is any pattern of from 1 to 11 bits specified by the programmer and used to check the contents of an information register. In most skip instructions, the CQ field is usually written to contain all zeros. The F bit (function) in the COMMAND field is used to distinguish between the two types of instructions. In this bit position a 1 specifies the SKF instruction and an 0 specifies the SKC instruction.

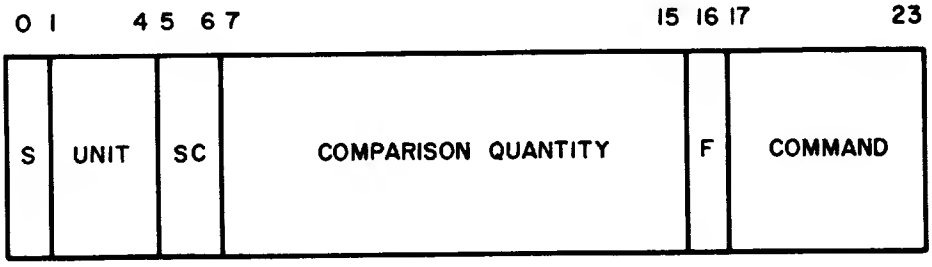


Figure TAC-18. Format of SKC and SKF Instructions

In the class of instructions where the S bit is zero, the SC field is used to further define the information register being interrogated as follows:

CODE	MEANING
00	Buffer-Controller or tape unit involved
01	Assembler unit or drum involved
10	Real Time device involved
11	Paper Tape System involved (not connected to IOB)

CODING SKIP INSTRUCTIONS

Skip instructions may be written by using either TAC mnemonic commands (i.e., the SKC and SKF instructions) or TAC skip macro-instructions. The macro-instructions are part of the Philco 2000 library of macro-instructions and have been developed to provide an easier and more accurate method of writing skip instructions.

The Skip instructions presently available which may be used to check the contents of information registers in the various I-O systems are summarized in table TAC-1. The table also lists the applicable macro-instruction, the information register being checked, the format of the address field, and the command code for the mnemonic instruction.

Mnemonic Commands

When the TAC mnemonic commands SKC and SKF are used, the address portions of these instructions are written as octal address. For example, the SKC instruction is used

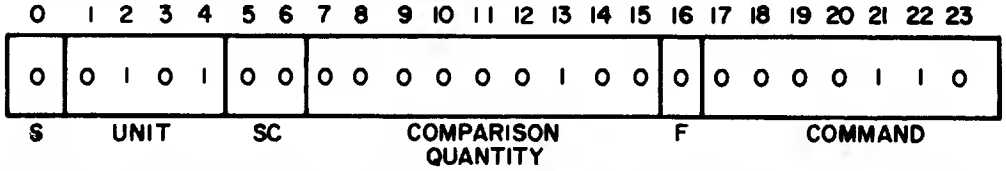
TABLE TAC-1
TABLE OF SKIP INSTRUCTIONS

SKIP MARCO-INSTRUCTION	I-O SYSTEM REGISTER CHECKED	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	
		S	UNIT				S	C	Comparison Quantity									F	COMMAND							
SKCA	IOP Assembler Counter	1	I-O CH				B	E	B	B	W	W	W	W	W	W	W	0	0	0	0	0	1	1	0	SKC
SKCUA	IOP Unit Availability	0	I-O CH				0	0	0	0	0	10	11	12	13	0	0	0	0	0	0	0	1	1	0	
SKCAA	IOP Assembler Availability	0	0	0	0	0	0	1	0	8	9	10	11	12	13	14	15	0	0	0	0	0	1	1	0	
SKCPT	Paper Tape Transmission	0	0	0	0	0	1	1	0	0	0	0	0	0	0	14	15	0	0	0	0	0	1	1	0	
SKCRTI	Real-Time Input	0	RT CH			1	1	0	0	0	0	0	11	12	13	0	0	0	0	0	0	0	1	1	0	
SKCRTO	Real-Time Output	0	RT CH			0	1	0	0	0	0	0	11	12	13	0	0	0	0	0	0	0	1	1	0	
SKFA	IOP Assembler Fault	1	I-O CH				0	1	7	8	9	10	11	0	13	14	15	1	0	0	0	0	1	1	0	SKF
SKFB	Buffer-Controller Fault	0	I-O CH				0	0	0	0	0	0	11	12	13	14	15	1	0	0	0	0	1	1	0	
SKFD	Drum Fault	0	0	0	0	0	1	1	0	0	0	0	0	0	0	14	15	1	0	0	0	0	1	1	0	
SKFPT	Paper Tape Fault	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	15	1	0	0	0	0	1	1	0	

to interrogate the IOP Unit Availability Register. The address of this instruction could be written as follows to specify tape unit 5 and to place a one in bit position 13 of the Comparison Quantity field:

SKC M/24004

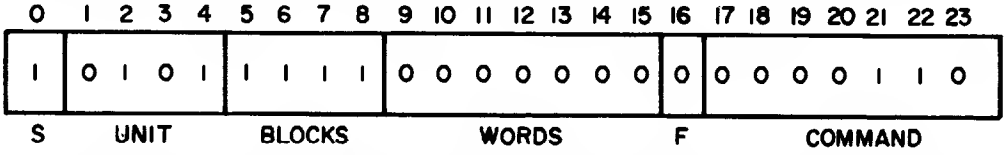
The relationship of the bit configuration in memory and the format of the applicable skip instruction listed in the table is illustrated below:



In the case where the IOP Assembler Counter is interrogated using a TAC mnemonic command, a one must be placed in the S bit position of the skip instruction. This can be accomplished by specifying the use of an index register even though these instructions are not indexable. For example, to specify tape unit 5 and to place one bits in positions 5 through 8 of the Comparison Quantity field when interrogating the IOP Assembler Counter Register, the address of the skip instruction could be written as follows:

SKC M/7600, 2X

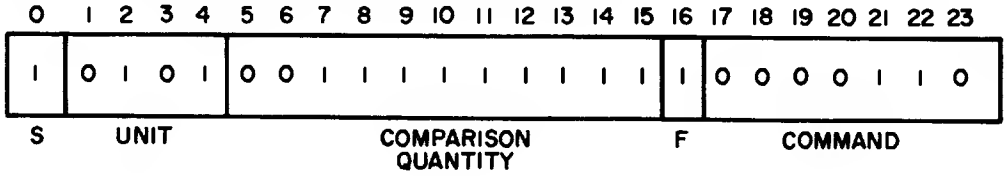
The relationship of the bit configuration in memory and the format of the applicable skip instruction listed in the table is illustrated below:



Another example of the S bit position of a skip instruction requiring a one bit is when the IOP Assembler Fault Register is checked. Suppose, for example, it is desired to check tape unit 5 and to place a zero in bit position 6 and one bits in positions 7 through 15. The coding could be as follows:

SKF M/4777, 2X

The relationship of the bit configuration in memory and the format of the applicable skip instruction listed in the table is illustrated below:



Skip Macro-Instructions

Skip macro-instructions provide the same checking capabilities as the TAC mnemonic commands, with less coding effort. When the macros are used, it is not necessary to specify the S bit or the SC field, because the name of the macro carries that significance. There is one exception, the SKCA macro. The requirements for using skip macro-instructions are that the UNIT field must be written first and in decimal form and then followed by the CQ field written in binary form. When the SKCA macro is written, the CQ field defining the blocks and words must be written in decimal form. In all cases, the parameters

in the address portion of the macro-instruction must be separated with semicolons. The following are examples of coding using skip macro-instructions which are based on the preceding examples of the mnemonic commands.

a. when checking the IOP Unit Availability Register

```
SKCUA        5; 0001$
```

b. when checking the IOP Assembler Counter Register

```
SKCA         5; 15; 0$
```

c. when checking the IOP Assembler Fault Register

```
SKFA         5; 0111111111$
```

It is possible to omit the CQ field when checking the contents of an information register for all zeros. In cases where the CQ field contains one or more one-bits, however, the field must be written out. With the exception of the SKCUA macro, zeros need not be written following ones in the CQ field.

RELATED INFORMATION REGISTERS

Each I-O system in the Philco 2000 contains one or more information registers which monitor the performance of the I-O system and the progress of data transmissions. Conditions in the systems are indicated with binary ones; a binary zero indicates the absence of a condition.

Registers in the IOP

There are four different information registers in the IOP, the Assembler Counter, Unit Availability, Assembler Availability, and the Assembler Fault Registers. The function of these registers is described in the chapter dealing with the IOP.

The SKCA instruction is used to check the contents of the Assembler Counter Register. The relationship between the bit positions of the register and the CQ field of the instruction is shown in figure TAC-19.

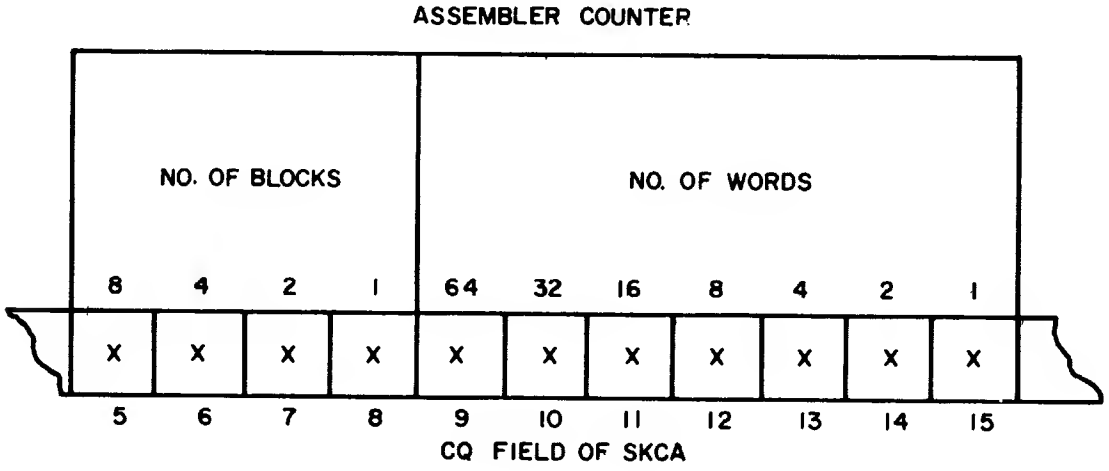


Figure TAC-19. Relation Between Assembler Counter and CQ Field of SKCA

The SKCUA instruction is used to check the contents of the Unit Availability Register. The relationship between the bit positions of the register and the CQ field of the instruction is shown in figure TAC-20. The condition which causes a 1 to be set in a bit position of the register is shown above that particular bit position.

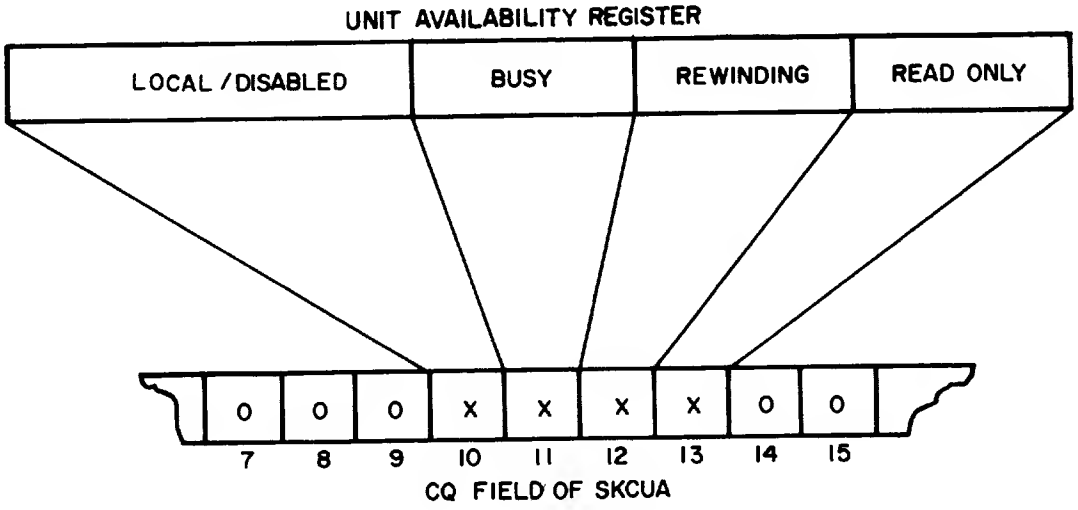
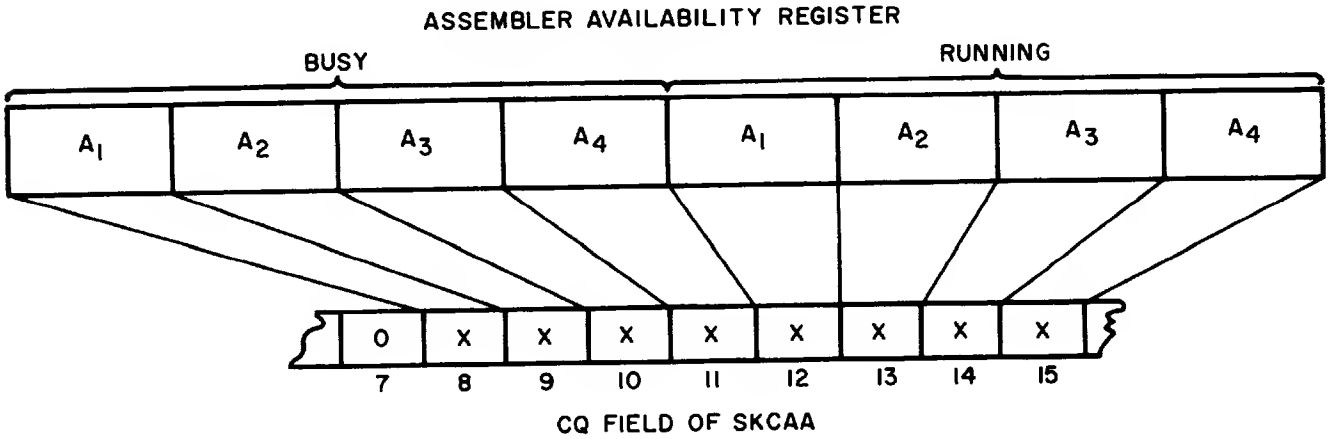


Figure TAC-20. Relation Between Unit Availability Register and CQ Field of SKCUA

The SKCAA instruction is used to check the contents of the Assembler Availability Register. The relationship between the bit positions of the register and the CQ field of the instruction is illustrated in figure TAC-24. The condition which causes a 1 to be set in a bit position of the register is shown above that particular bit position.



TAC-21. Relation Between Assembler Availability Register and CQ Field of SKCAA

The SKFA instruction is used to check the contents of the Assembler Fault Register. The relationship between the bit positions of the register and the CQ field of the instruction is illustrated in figure TAC-22. The condition which causes a 1 to be set in a bit position of the register is shown above that particular bit position.

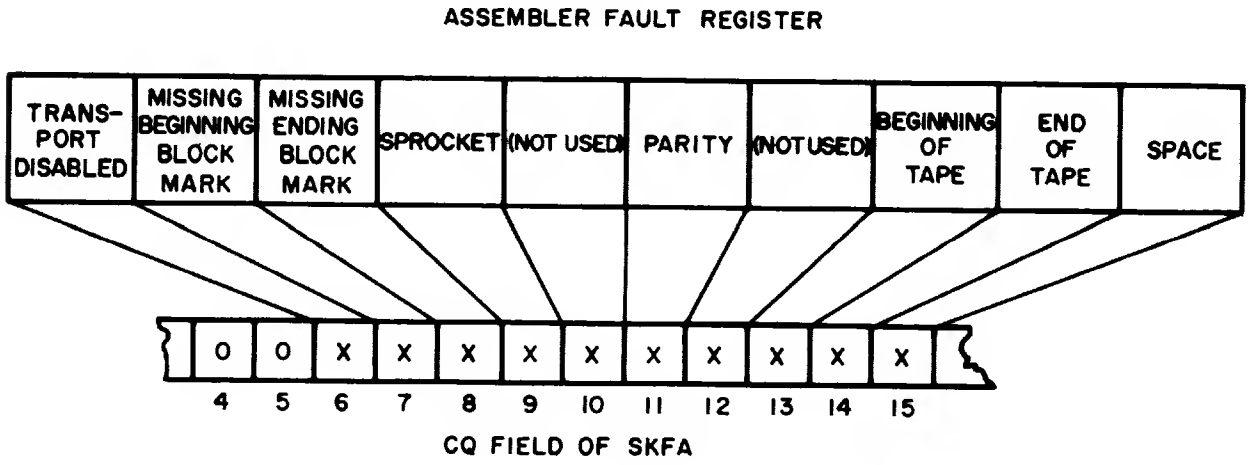


Figure TAC-22. Relation Between Assembler Fault Register and CQ Field of SKFA

Register in the UBC

There is one information register in the UBC, called the Buffer Fault Register. The function of this register is described in the chapter dealing with the UBC. The SKFB instruction is used to check the contents of the UBC. The relationship between the bit positions of the register and the CQ field of the instruction is illustrated in figure TAC-23. The condition which causes a 1 to be set in a bit position of the register is shown above that particular bit position. At present, the UBC Mechanical Fault indicator is not used.

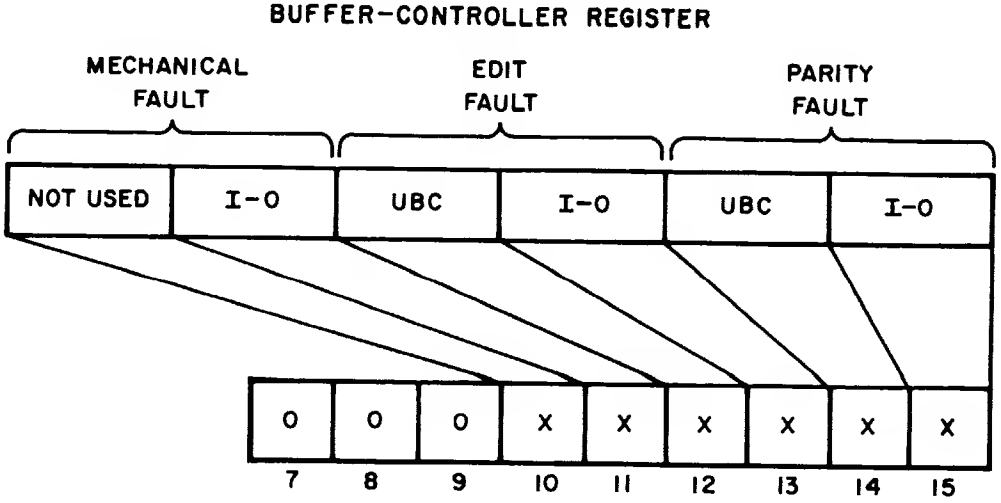


Figure TAC-23. Relation Between Buffer-Controller Register and CQ Field of SKFB

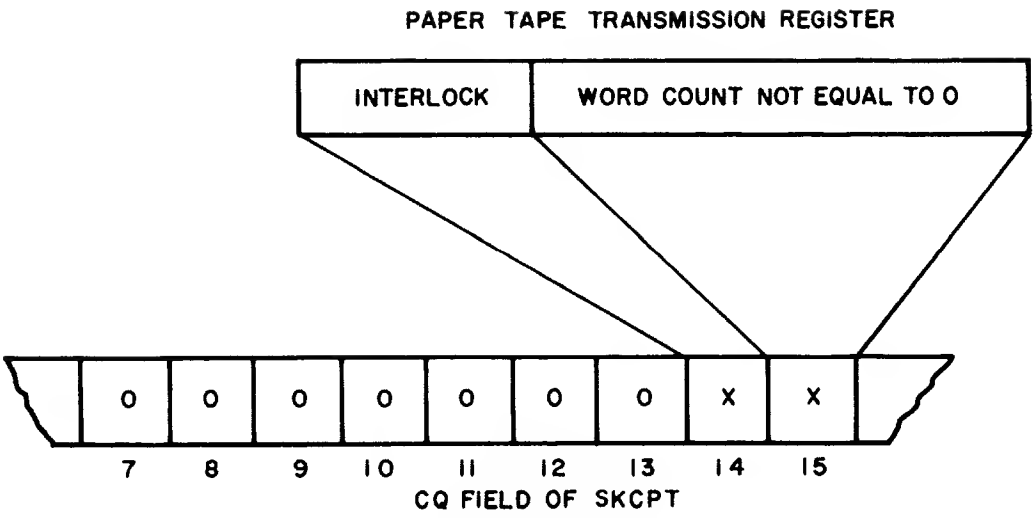


Figure TAC-24. Relation Between Paper Tape Transmission Register and CQ Field of SKCPT

Registers in the Paper Tape System

There are two information registers in the Paper Tape System, called the Paper Tape Transmission and Paper Tape Fault Registers. The function of these registers is described in the chapter dealing with the Paper Tape System.

The SKCPT instruction is used to check the contents of the Paper Tape Transmission Register. The relationship between the bit positions of the register and the CQ field of the instruction is illustrated in figure TAC-24. The condition which causes a 1 to be set in a bit position of the register is shown above that particular bit position.

The SKFPT instruction is used to check the contents of the Paper Tape Fault Register. The relationship between the bit positions of the register and the CQ field of the instruction is contained in figure TAC-25. The condition which causes a 1 to be set in a bit position of the register is shown above that particular bit position.

Register in the Magnetic Drum System

There is one information register in the Magnetic Drum System, called the Drum Fault Register. The function of this register is described in the chapter dealing with the Magnetic Drum System.

The SKFD instruction is used to check the contents of the Drum Fault Register. The relationship between the bit positions of the register and the CQ field of the instruction is shown in figure TAC-26. The condition which causes a 1 to be set in a bit position of the register is shown above that particular bit position.

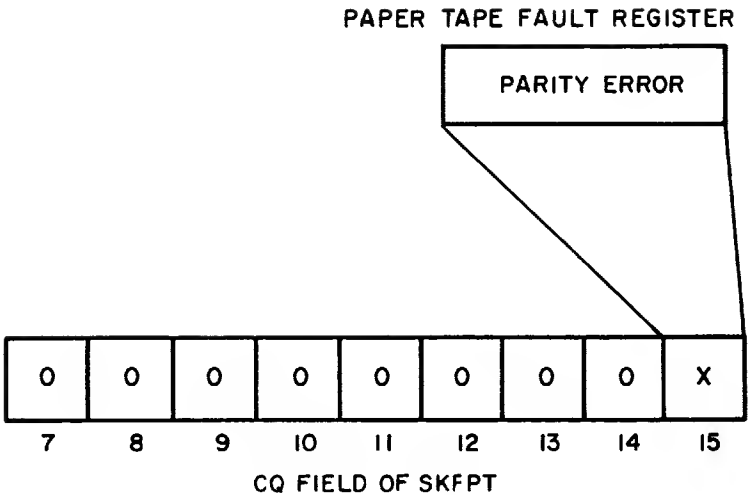


Figure TAC-25. Relation Between Paper Tape Fault Register and CQ Field of SKFPT

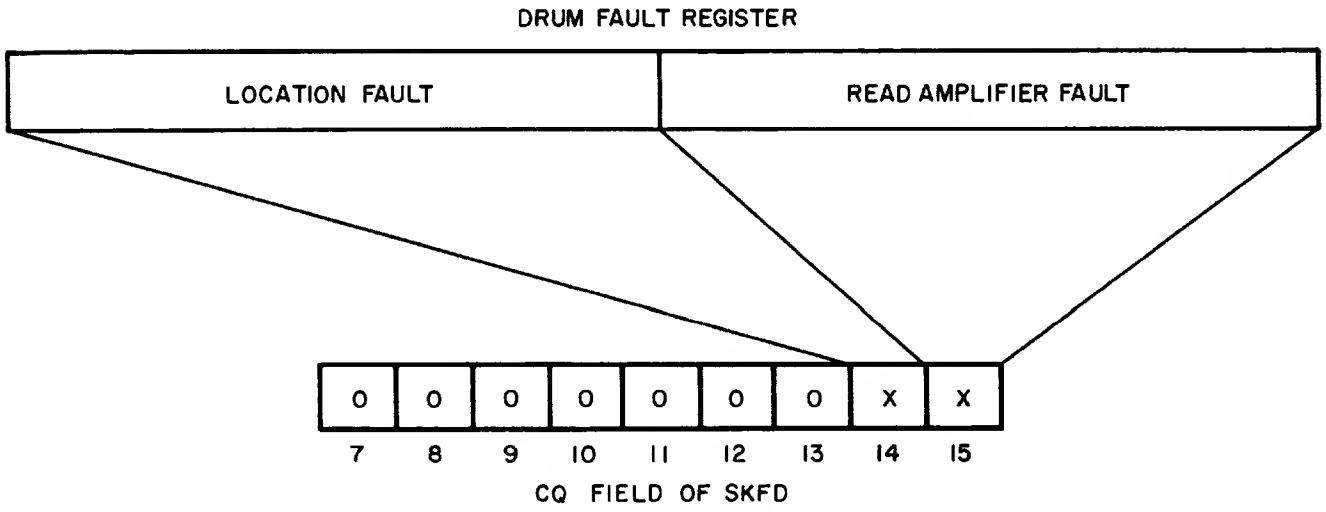


Figure TAC-26. Relation Between Drum Fault Register and CQ Field of SKFD

Registers in the Real-Time System

Each real-time device connected to the Real-Time Scanner contains an information register which displays the status of that device and the progress of data transmissions through it. There are two special skip instructions used with the scanner to check the contents of this register. They are the SKCRTI, and SKCRTO instructions, and are defined as follows:

a. SKCRTI, checks the availability of a unit to accept an RDDRT order

b. SKCRTO, checks the availability of a unit to accept a WRRT order

The relationship between the bit positions of the register and the CQ field of these instructions is contained in figure TAC-27. The condition which causes a 1 to be set in a bit position of the register is shown above that particular bit position.

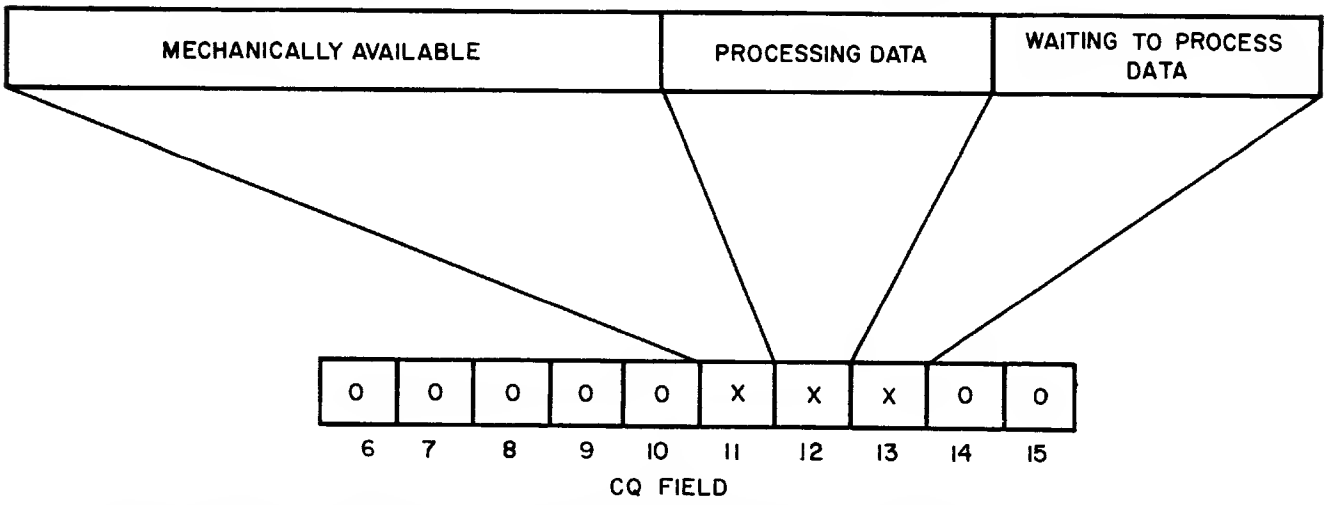


Figure TAC-27. Relation Between Real-Time System and CQ Field of Real-Time Skip Instructions

INTRODUCTION TO INPUT-OUTPUT MACRO-INSTRUCTIONS

Input-output macro-instructions have been developed to provide an accurate, easier, and more efficient method of initiating I-O processing operations. Instead of forming an I-O order using a TAC constant and then writing the Skip instructions necessary to determine the availability of the object I-O system before executing that order, the programmer is permitted to perform the same operation by using an input-output macro-instruction. Macro-instructions allow I-O orders to be stored and their execution to be controlled automatically by an executive subroutine. This method of coding insures that the order will be executed whenever the I-O system can accept that order; meanwhile, the Central Computer can continue with processing operations.

The macro-instruction is defined as a TAC instruction which causes a previously prepared and stored series of instructions to be placed into the program at the point where the macro-instruction is written. The series of instructions that replaces the macro-instruction is called the macro-expansion. In the case of I-O macro-instructions, each expansion begins with a jump instruction which is followed by one or more halt instructions. The ADDRESS field of the halt instructions contains parameters that are used to form the I-O order.

Input-output macro-instructions are identified with mnemonic commands and have one or more parameters. For example, the macro-instruction to read magnetic tape forward is RDMTF, and the parameters of that order are as follows:

UNIT; the tape unit involved

CSA; core starting address

NBP; number of blocks to be processed

NBS; number of blocks to be spaced

CODING PROCEDURE

A macro-instruction is written by placing its name in the COMMAND field and its parameters in the ADDRESS field. When more than one parameter is required, the parameters must be separated with semicolons. For example, the magnetic tape macro-instruction to space 10 blocks and then read 10 blocks from Magnetic Tape Unit Number 2, starting with memory location $(1000)_8$ would be written as follows:

```
RDMTF    N/2T23; M/1000; 10; 10$
```

(The first parameter of this macro can be written either as a pool or non-pool constant scaled at T23. In the example, a pool constant is used.)

When the program is compiled by TAC, the macro-expansion that replaces the instruction would be as follows:

```
JMP     PROC.          RDMTF $
HLT     N/2T23 $ UNIT
HLT     M/1000 $ CSA
HLT     10 $ NBS
HLT     10 $ NBP
```

The macro-expansion begins with a jump instruction to the subroutine for magnetic tape and to the point in that subroutine which will cause the read order to be fabricated. The halt instructions that follow the jump contain the parameters of the read order.

Following the jump to the designated point in the subroutine, instructions in the subroutine extract the parameters of the order from the ADDRESS fields of the halt instructions and compose the 48 bit I-O order. After the order has been formed, the decision to execute it is made by another subroutine, called PROC.

PROC is an executive routine that stores I-O orders and determines at what point in the program an I-O order will be executed. After the I-O order has been formed by the processing routine, a jump is made from that routine to PROC. In PROC, the I-O order is noted, and the list of stored orders is then examined. If any order can be executed, control is returned by PROC to the appropriate processing routine which will execute that order. Whenever control is passed to PROC, as many orders as can be accepted by the I-O systems will be executed.

Stored orders are executed in the sequence in which they appear in the list; however, an I-O order will be executed before others when the orders before it are for units which have an order outstanding.

PROC is part of the Philco 2000 library and must be initialized before it can be used. The INIT macro-instruction performs this function, and it must be executed at least once in the program preceding the coding of I-O macro-instructions. This macro clears PROC's list of stored orders, and establishes the error exit point for the system.

The INIT macro has two parameters: N and SYSTEM ERROR. The N parameter specifies the number of orders which can be stored in PROC's list at any one time, and this number is fixed at 16.

The SYSTEM ERROR parameter is the symbolic address to which PROC will jump if the list of stored orders is full and another macro-instruction whose order must be stored is executed, or if an error occurs such as checking out of sequence, tape unit not write enabled, tape in local, etc.

In a program containing 10 I-O orders, the INIT macro-instruction may be written as follows:

L	LOCATION	COMMAND	ADDRESS AND REMARKS
I		ABC	
		AFEND	80$
		NAME	PHILCØ
		INIT	16; END

L	LOCATION	COMMAND	ADDRESS AND REMARKS
		.	
		.	
		.	
		.	
	END	HLT	Ø/7777

CHECKING MACRO-INSTRUCTIONS

Checking macro-instructions have been provided to check I-O orders for completion, and it is the usual practice to follow I-O macro-instructions with a checking macro. In addition to causing the order to be checked for completion, the checking macro also causes the I-O order to be removed from PROC's list of stored orders when that order has been completed.

An example of one type of checking macro is CHKCOMP. It consists of the name and three parameters, which are LOCATION, INCOMPLETE, and ERROR. The LOCATION parameter is the address of the macro-instruction whose I-O order is being checked; the INCOMPLETE parameter is the address to which PROC will return if the I-O order has not been completed. Otherwise, PROC will return to the first instruction following the last parameter of the macro-expansion. The ERROR parameter is the address to which PROC will return if the execution of the I-O order has resulted in some type of error (parity, edit, mechanical).

CHKCOMP may be used, for example, following a RDMTF macro-instruction, and the coding in this case may be as follows:

LOCATION	COMMAND	ADDRESS AND REMARKS
ABLE	RDMTF	UNIT; CSA; NBP; NBS$
BAKER	CHKCØMP	ABLE; BAKER; DIAGNØ$
	.	
	.	
	.	
DIAGNØ	ERRØRS	FINAL ERROR ADDRESS$

ERRORS MACRO-INSTRUCTION

The ERRORS macro-instruction allows a jump to be made to an error correcting routine in PROC, called ERRSUB, which will attempt to complete interrupted orders resulting from parity or sprocket errors. When the ERRORS macro is executed, ERRSUB searches the list of stored orders for any incomplete orders. When an incomplete order is detected, ERRSUB interrogates the fault register of the I-O system and if a parity or sprocket error condition is present, attempts to correct it. If any error other than parity or sprocket is detected, the subroutine jumps to the location specified in the address field of the ERRORS macro-instruction.

The ERRORS macro-instruction consists of the mnemonic command and one parameter, and is written as follows:

ERRORS FINAL ERROR ADDRESS

The FINAL ERROR ADDRESS is any symbolic address to which the subroutine ERRSUB will jump if either of the following conditions are present:

a. if any transmission error other than a parity or sprocket error is present
b. if a parity or sprocket error was detected and five unsuccessful attempts have been made to reread or to rewrite the block in which the error occurred.

(In both of the above cases, space errors are ignored.)

The ERRORS macro may appear at any point in the program, and no attempt is made to execute anv orders in the list of stored orders when ERRORS is being executed.

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